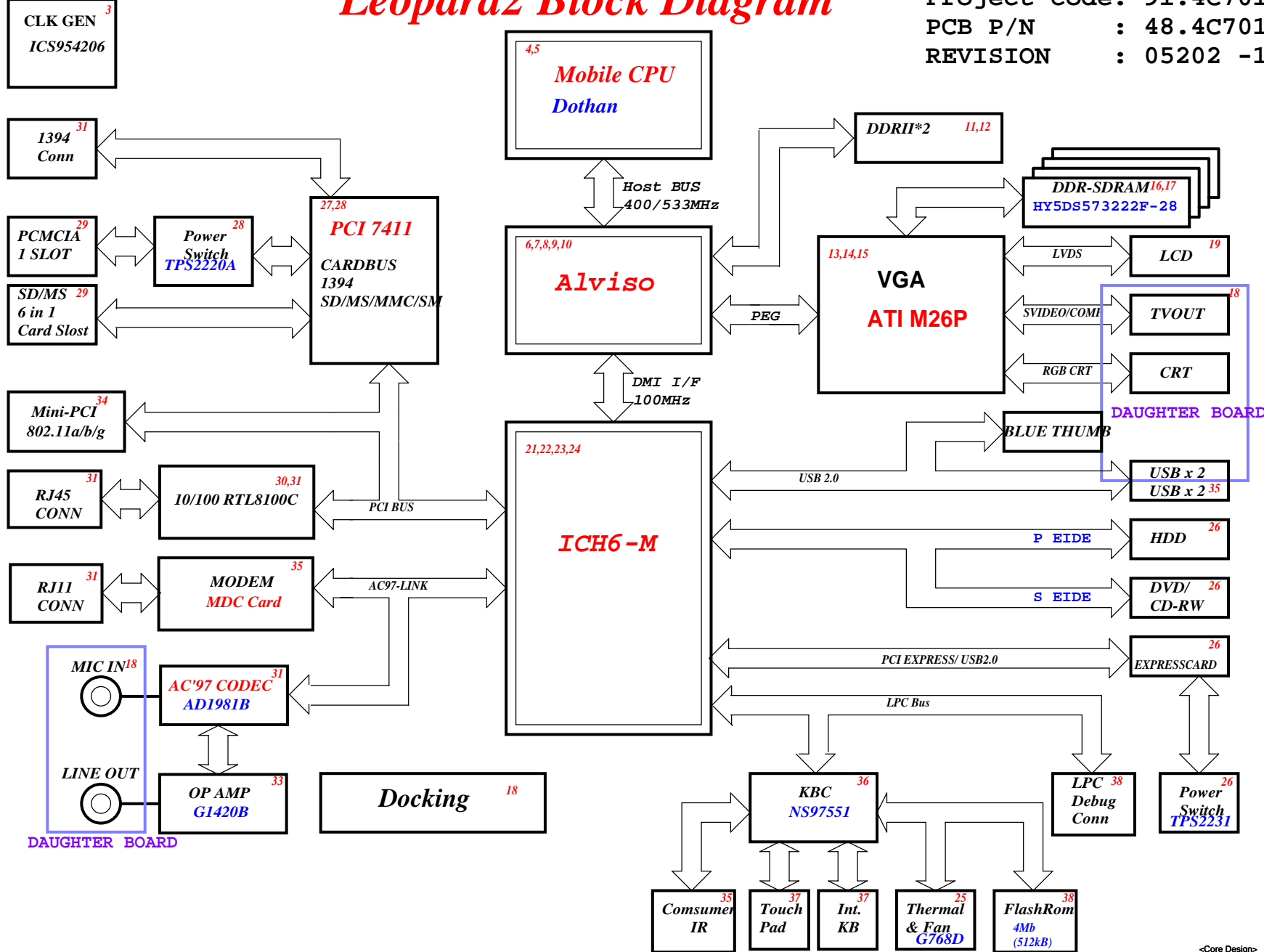


# Leopard2 Block Diagram

Project code: 91.4C701.001  
PCB P/N : 48.4C701.011  
REVISION : 05202 -1



SYSTEM DC/DC TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 5V_S3 3V_AUX

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_VGA_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram  
Size: A3 Document Number: Leopard2  
Date: Monday, July 11, 2005 Sheet 1 of 47 Rev: -1

ICH6-M Integrated Pull-up  
and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDRQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series  
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V\_S0= 5 Voltage power up on system work(S0 state)  
5V\_S3= 5 Voltage suspend to RAM(S3 state)  
5V\_S5= 5 Voltage soft off(S5 state)  
3D3V\_S0= 3.3 Voltage power up on system work(S0 state)  
3D3V\_S3= 3.3 Voltage suspend to RAM(S3 state)  
3D3V\_S5= 3.3 Voltage soft off(S5 state)  
LVDDR\_2D8V= 2.8 Voltage power up on system work(S0 state)  
1D8V\_S3= 1.8 Voltage suspend to RAM(S3 state)  
2D5V\_S0= 2.5 Voltage power up on system work(S0 state)  
  
VCC\_CORE\_S0= CPU VID Voltage power up on system work(S0 state)  
1D5V\_VCCA\_S0= 1.5 Voltage power up on system work(S0 state)  
1D5V\_S0= 1.5 Voltage power up on system work(S0 state)  
1D5V\_S5= 1.5 Voltage soft off(S5 state)  
DDR\_VREF= 0.9 Voltage power up on system work(S0 state)  
1D2V\_VGA\_S0= 1.2 Voltage power up on system work(S0 state) for VGA  
VRAM\_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM  
1D05V\_S0= 1.05 Voltage power up on system work(S0 state)  
CORE\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power  
VCCP\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

<Core Design>

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Title

ITP

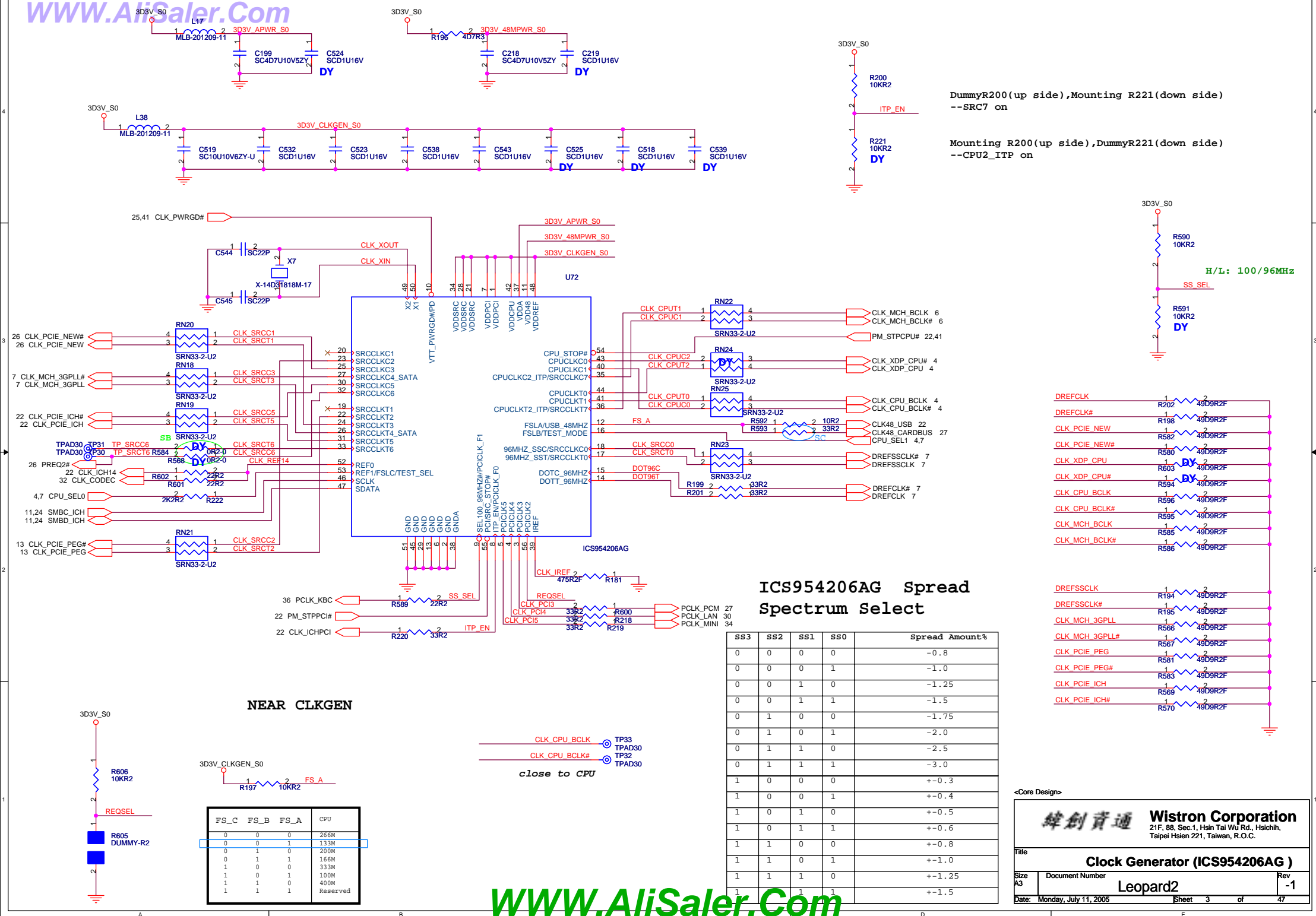
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A3

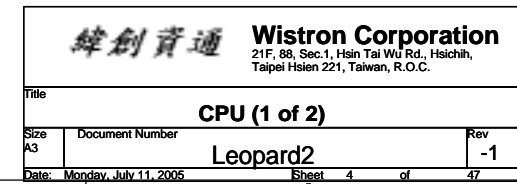
Document Number  
Leopard2

Rev  
-1

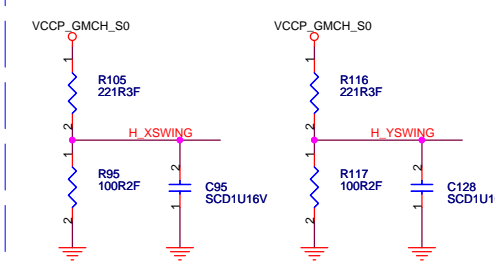
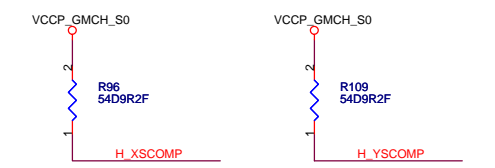
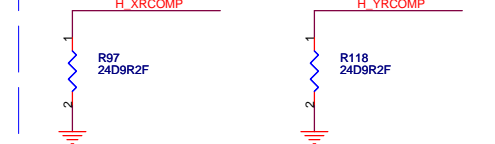
Date: Wednesday, July 06, 2005

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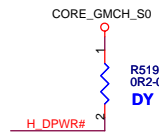
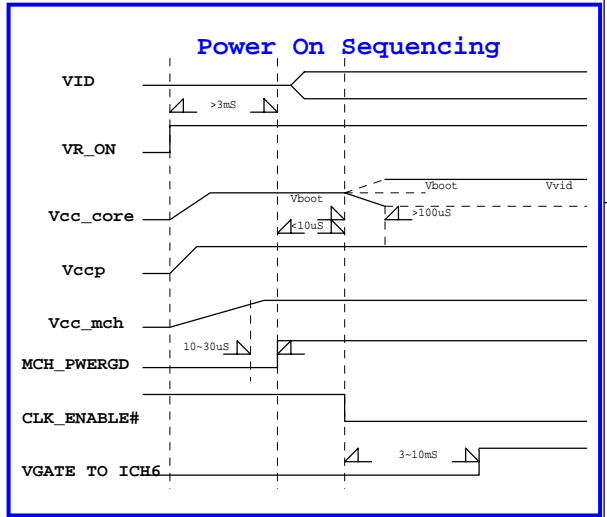
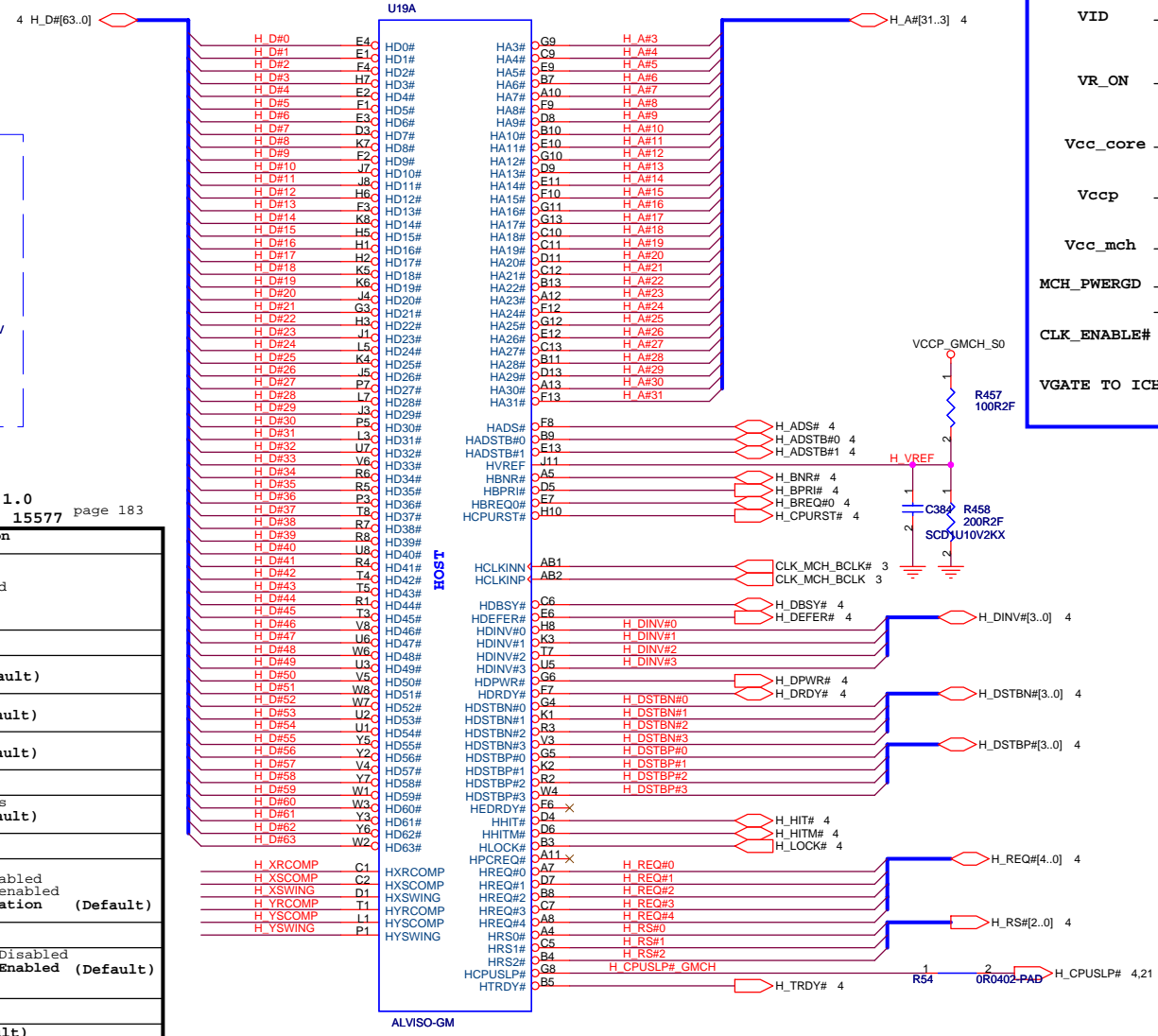
Trace 10 mil wide with 20 mil spacing

## Alviso Strapping Signals and Configuration

REV.NO. 1.0  
REF. NO. 15577 page 183

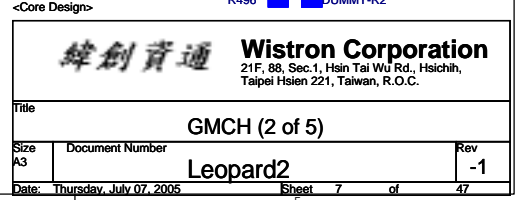
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 1 = DDR1 (Default)
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

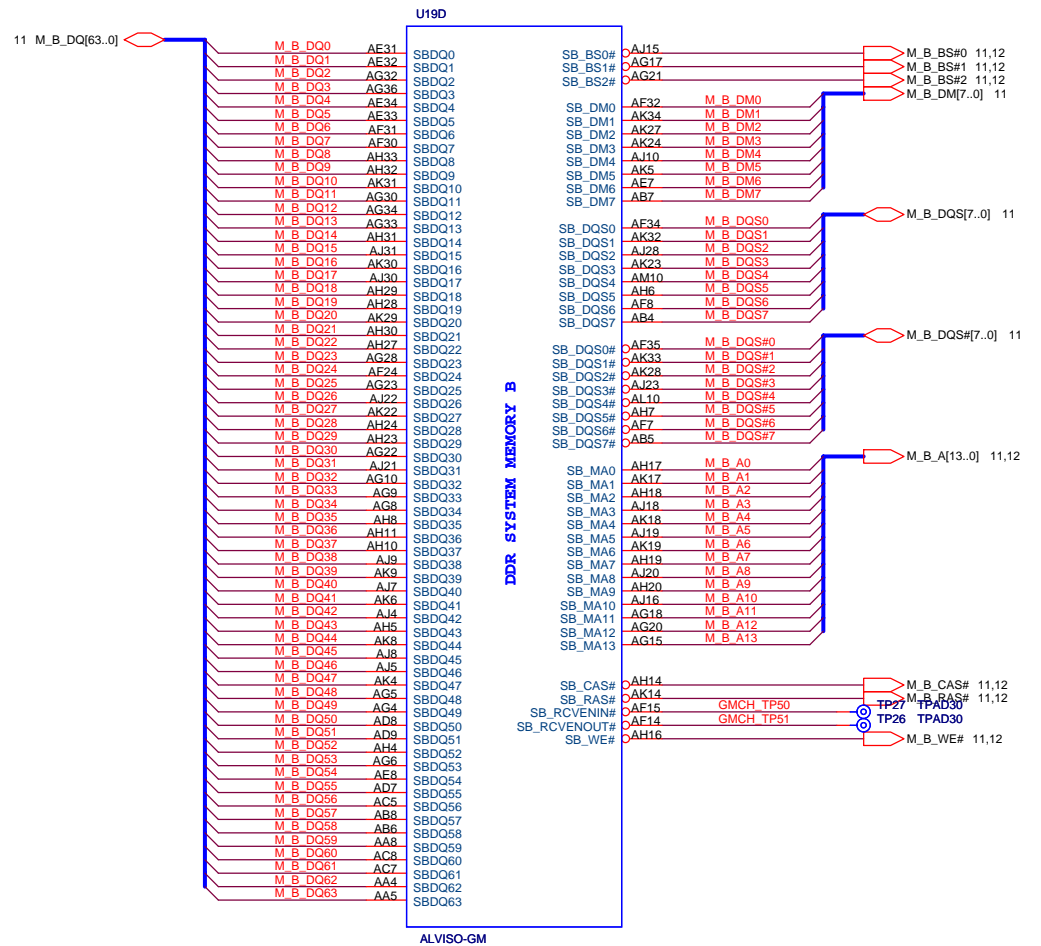
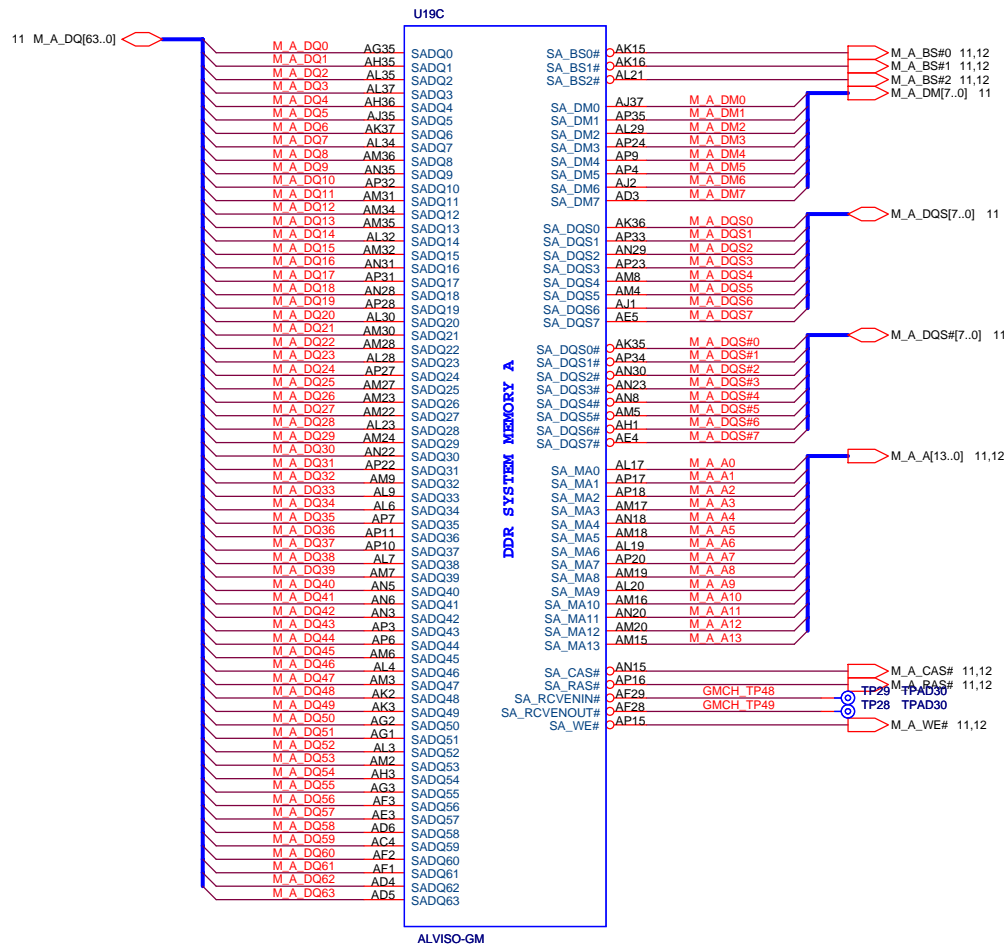
NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX in signal.



ALVISO-GM:71.0GMCH.08U  
ALVISO-PM:71.0GMCH.0BU  
ALVISO-GML:71.0GMCH.0JU



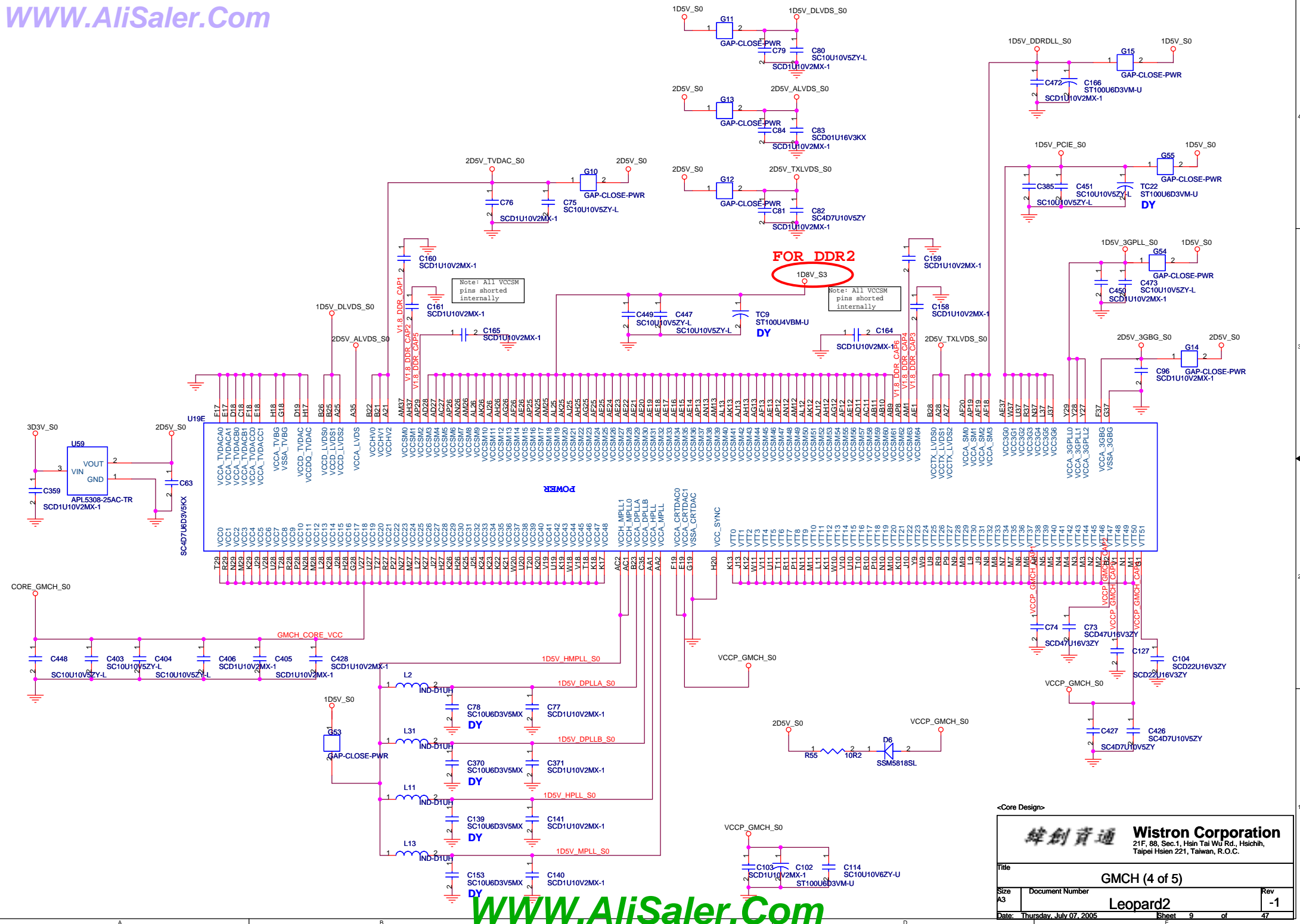


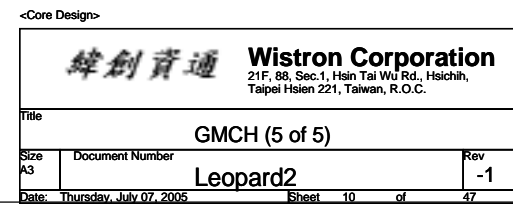


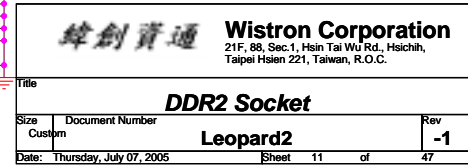
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<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: <b>GMCH (3 of 5)</b></p>		
Size: A3	Document Number: <b>Leopard2</b>	Rev: <b>-1</b>
Date: Thursday, July 07, 2005	Sheet: 8	of 47

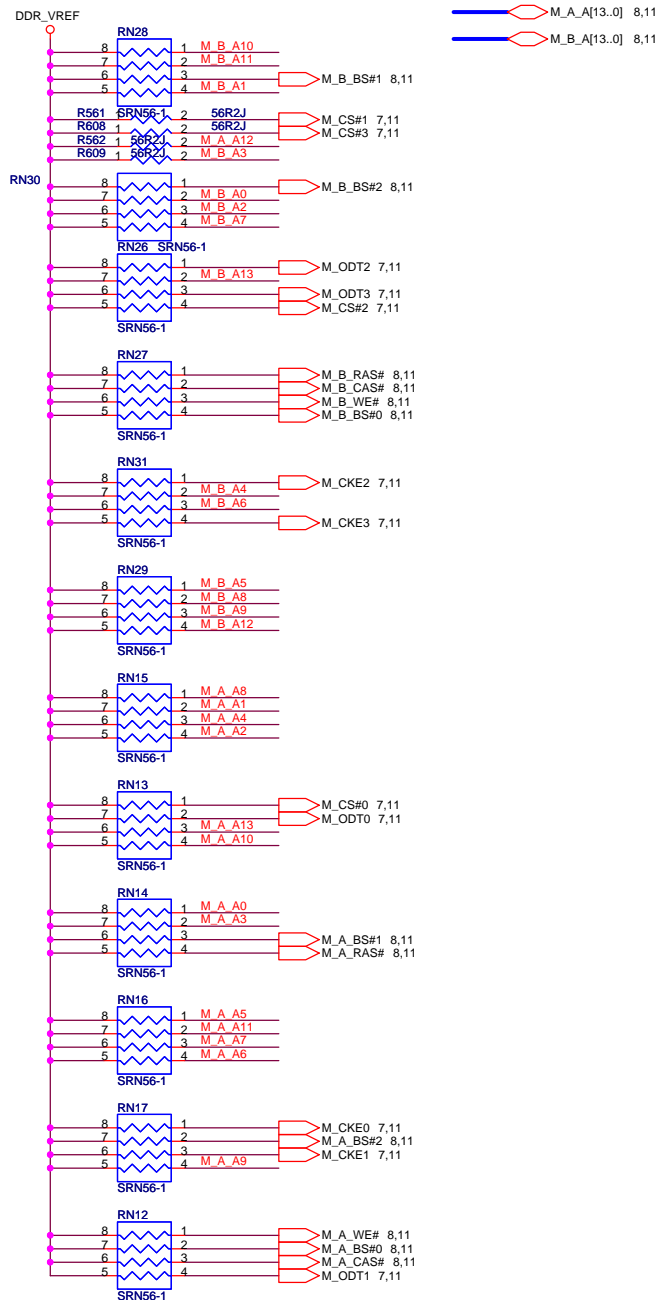






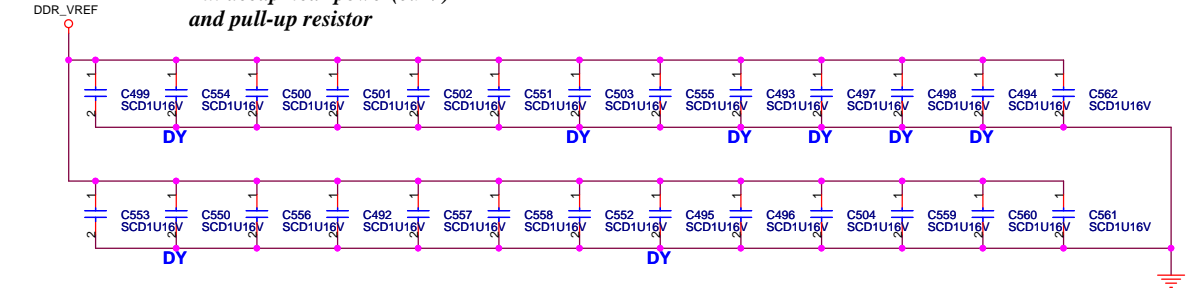


Put decap near power(0.9V) and pull-up resistor

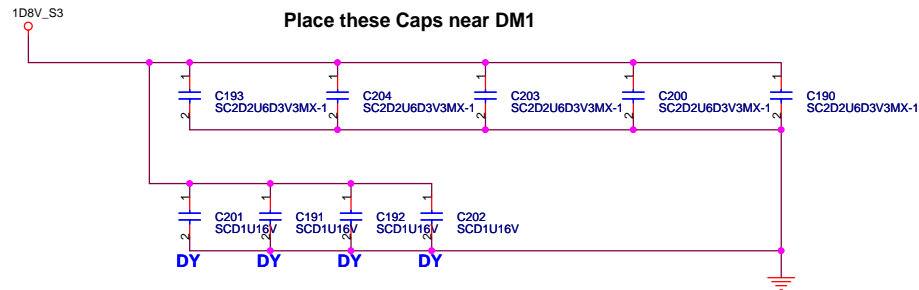


## Decoupling Capacitor

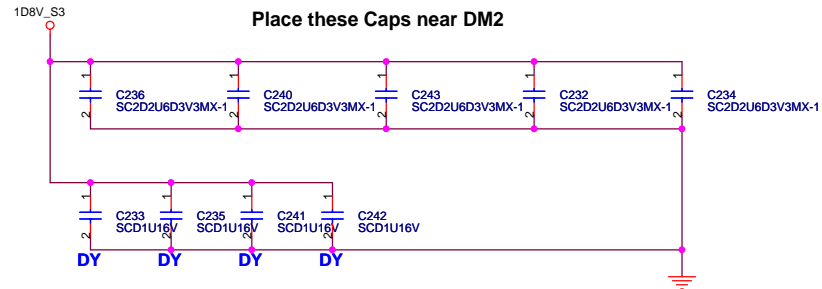
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2

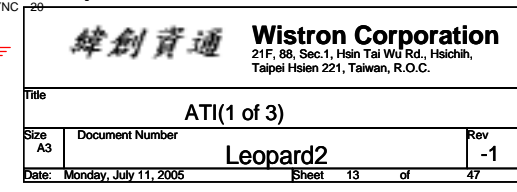


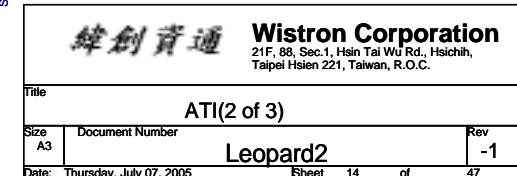
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緯創資通

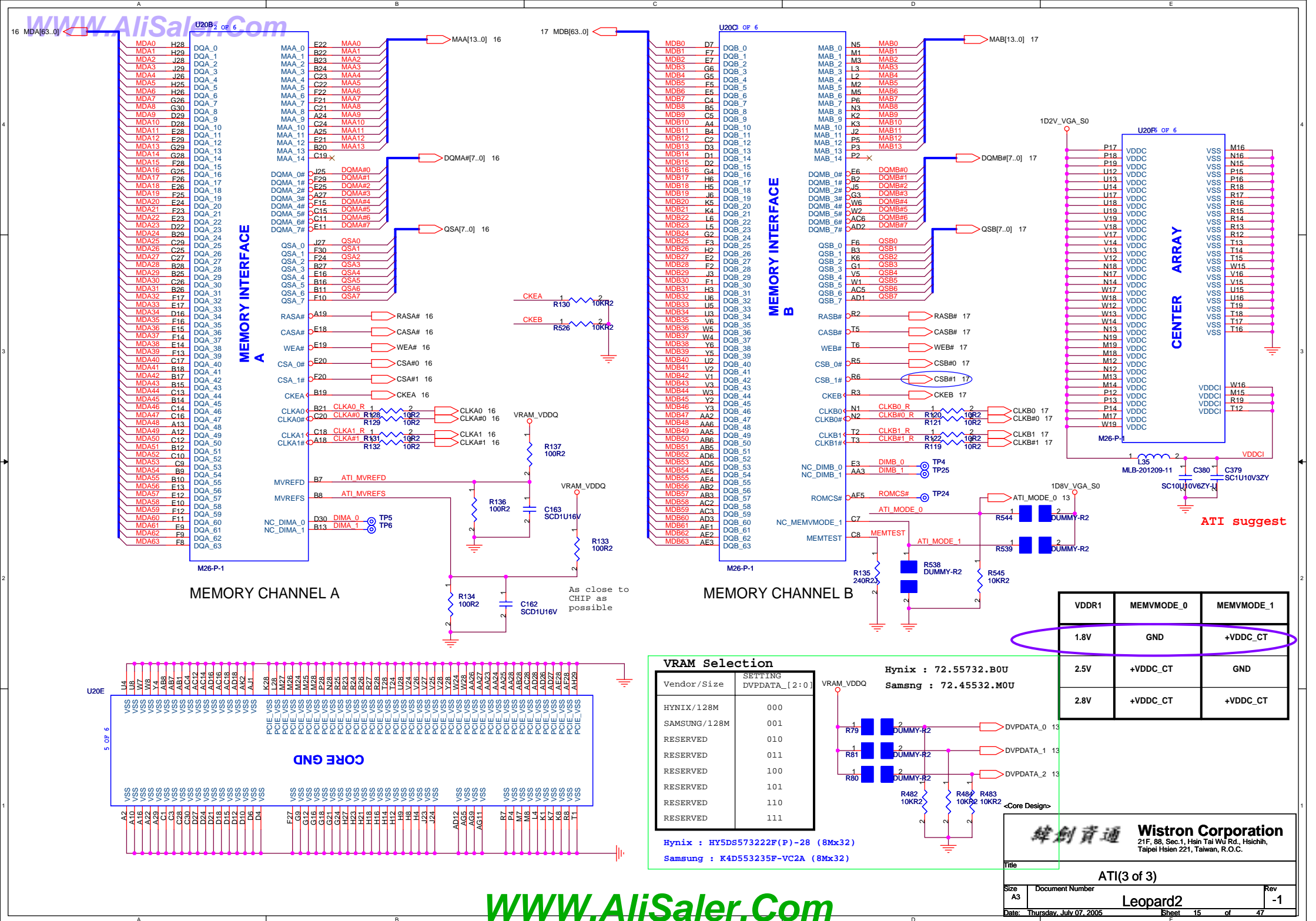
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Taipei Hsien 221, Taiwan, R.O.C.

Title		DDR2 Termination Resistor	
Size	A3	Document Number	Leopard2
Date:	Thursday, July 07, 2005	Sheet	12 of 47
Rev	-1		



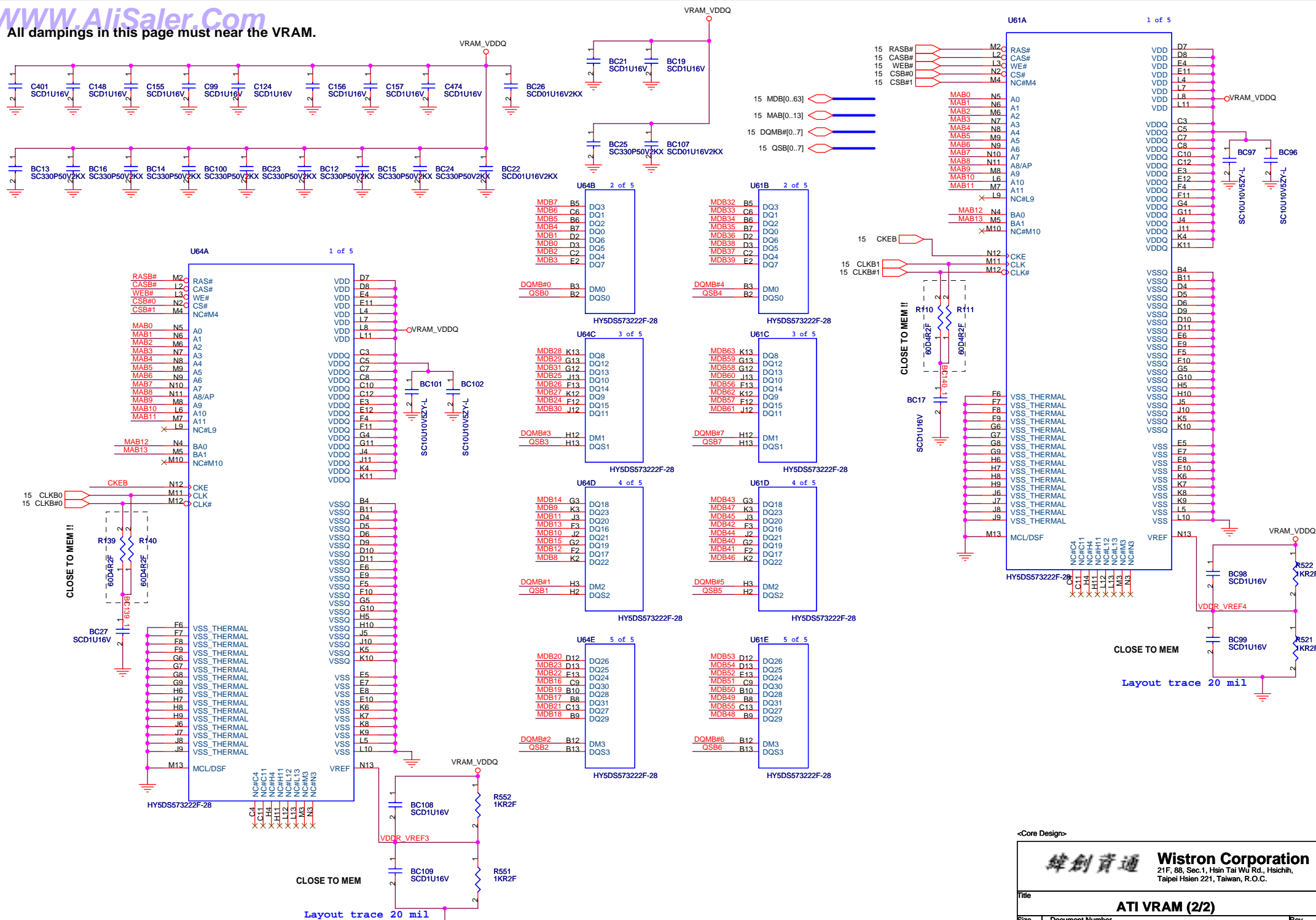


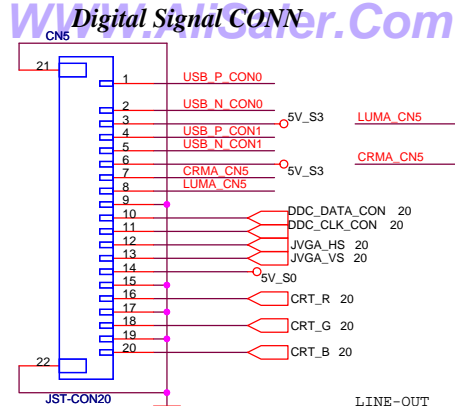




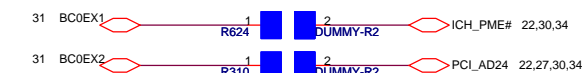
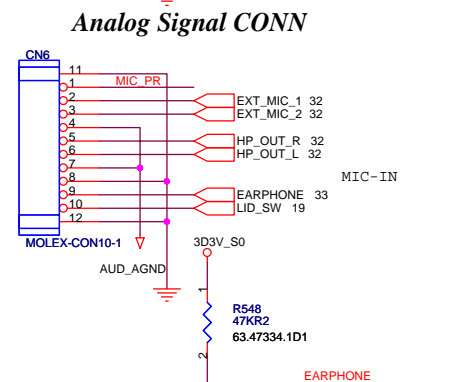
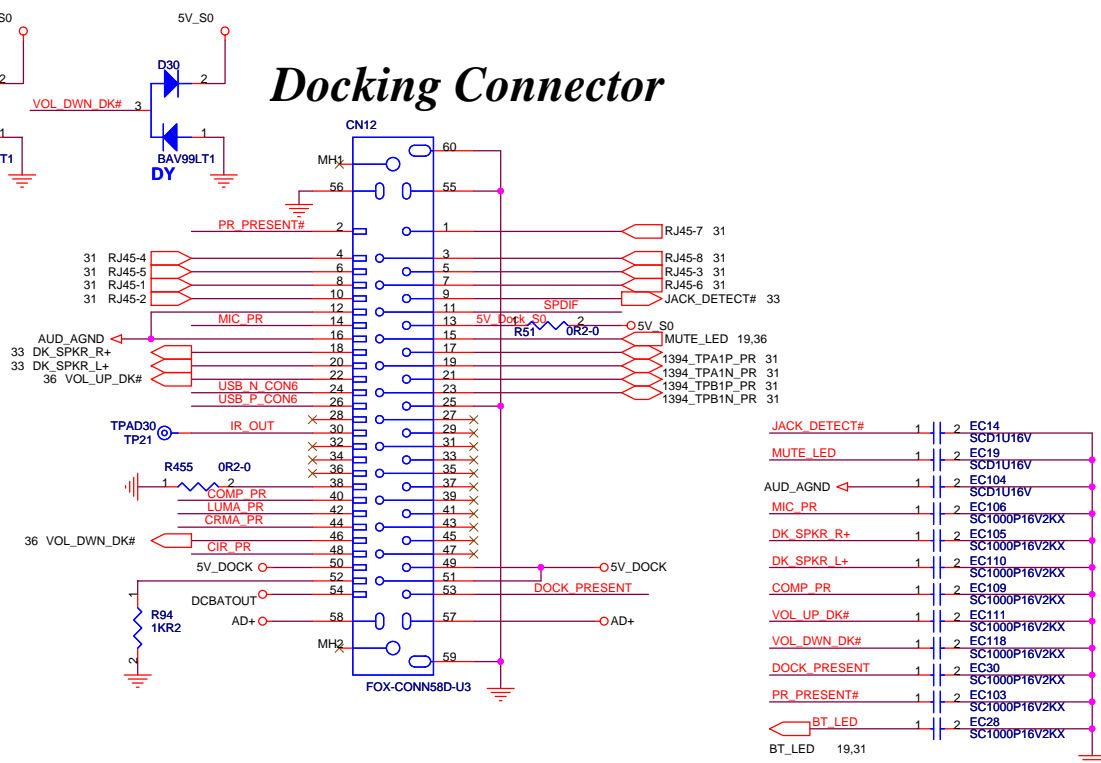
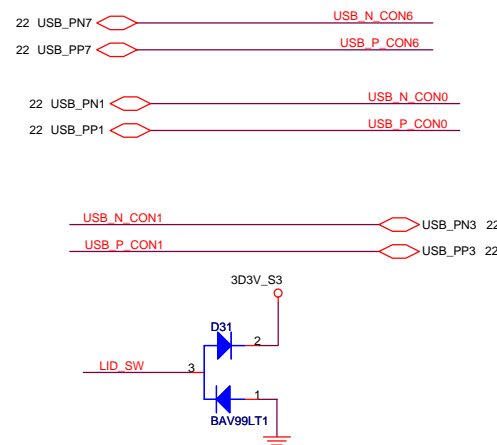


47



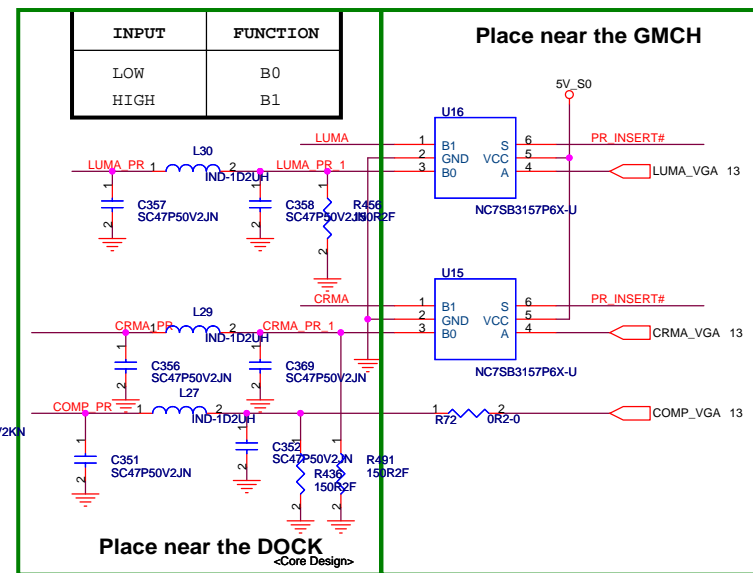
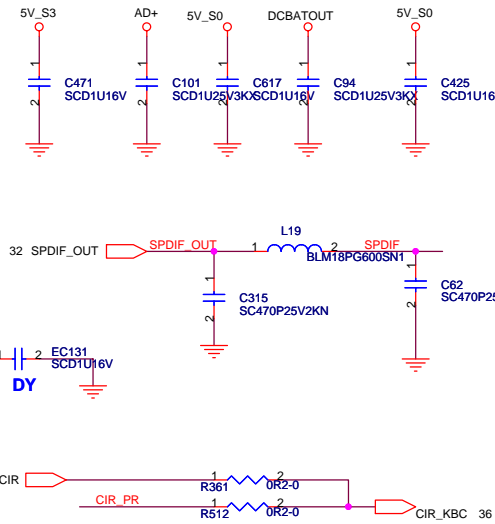
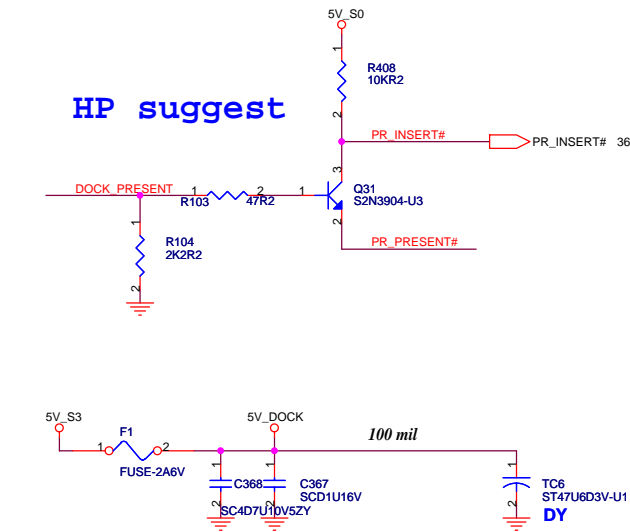


### Close to Docking CN

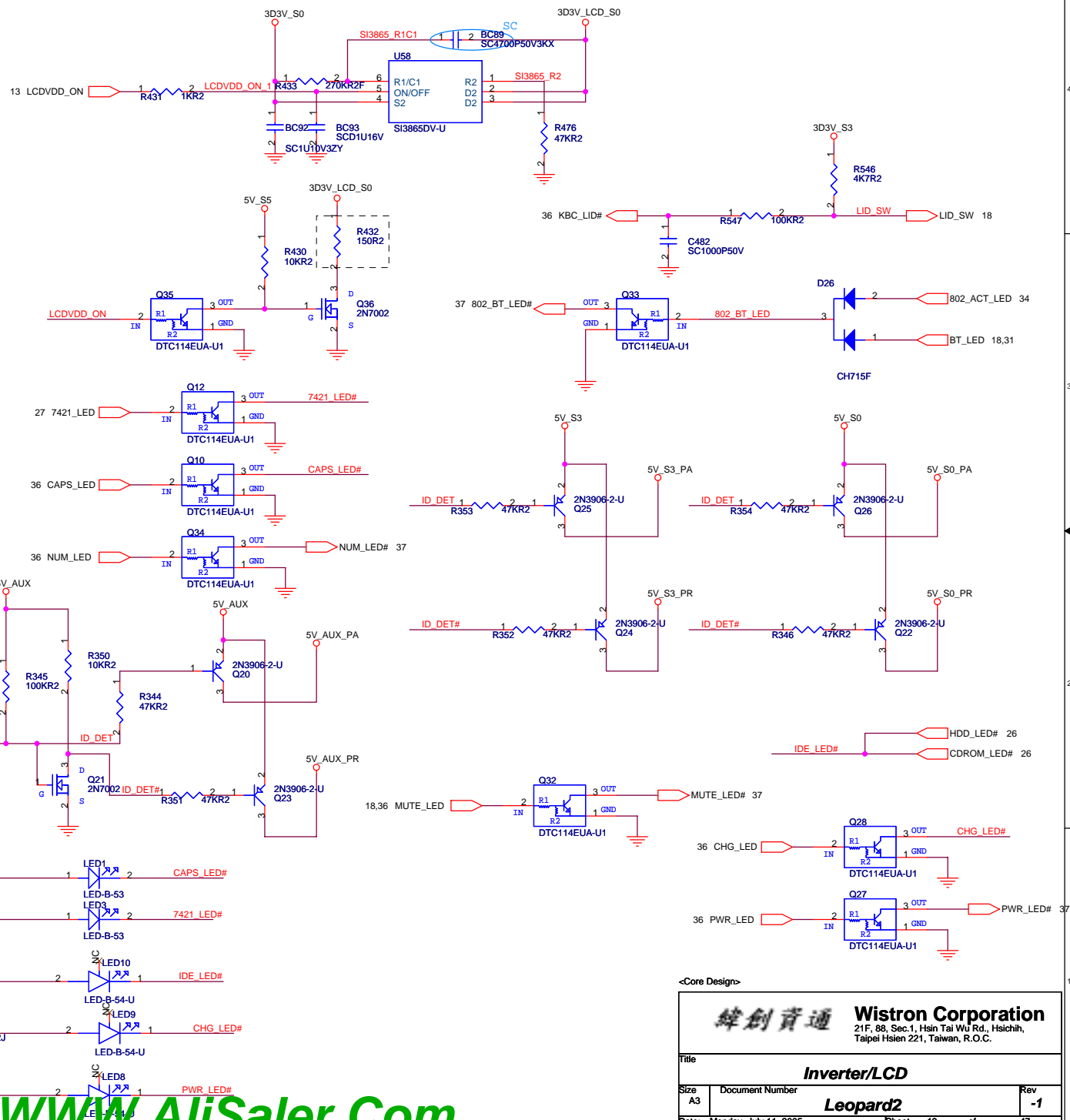
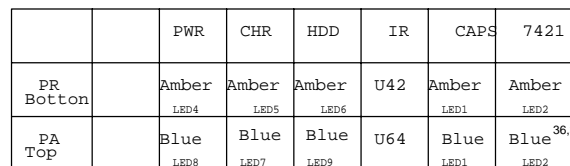


Please close to ICH6

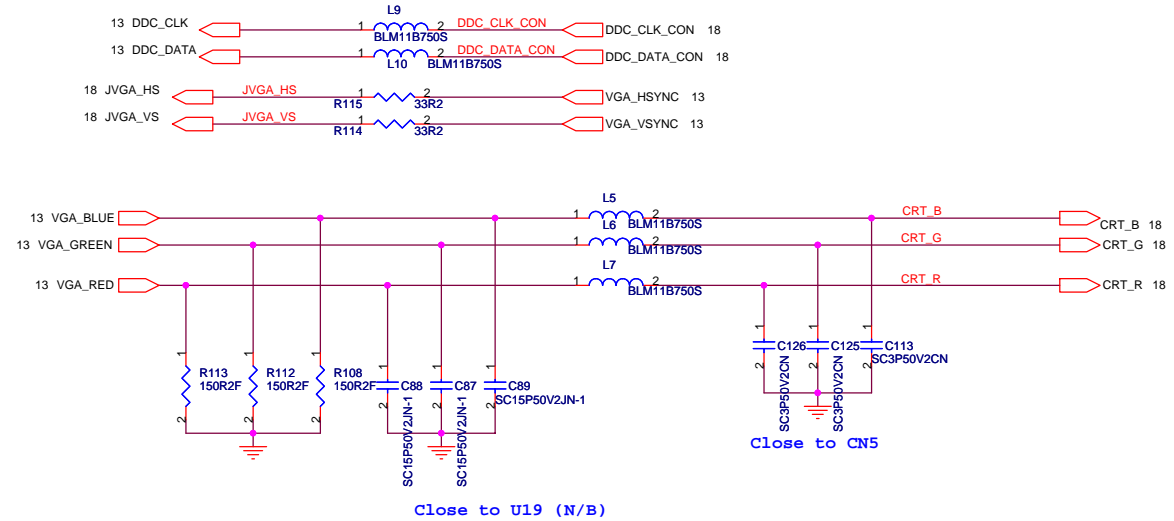
HP suggest



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Taipei Hsien 221, Taiwan, R.O.C.

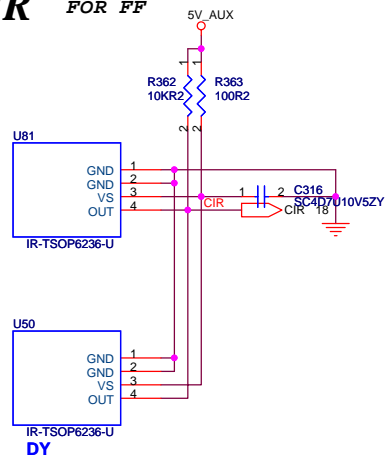


# CRT



010804 Modified on Astro ID request

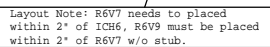
## CIR FOR FF

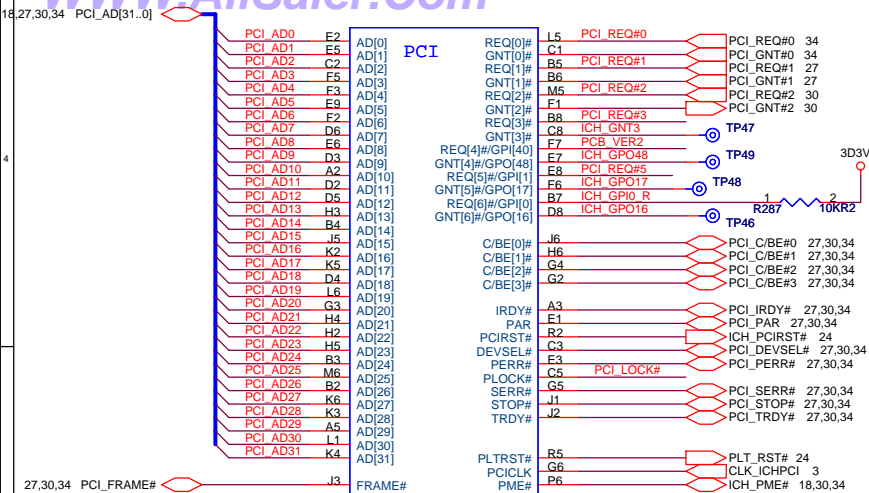


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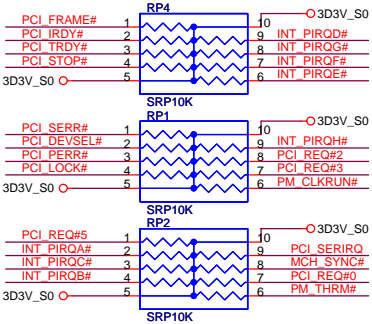
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CRT/ CIR	
Size	Document Number	Rev	
A3		Leopard2	-1
Date: Thursday, July 07, 2005		Sheet	20 of 47







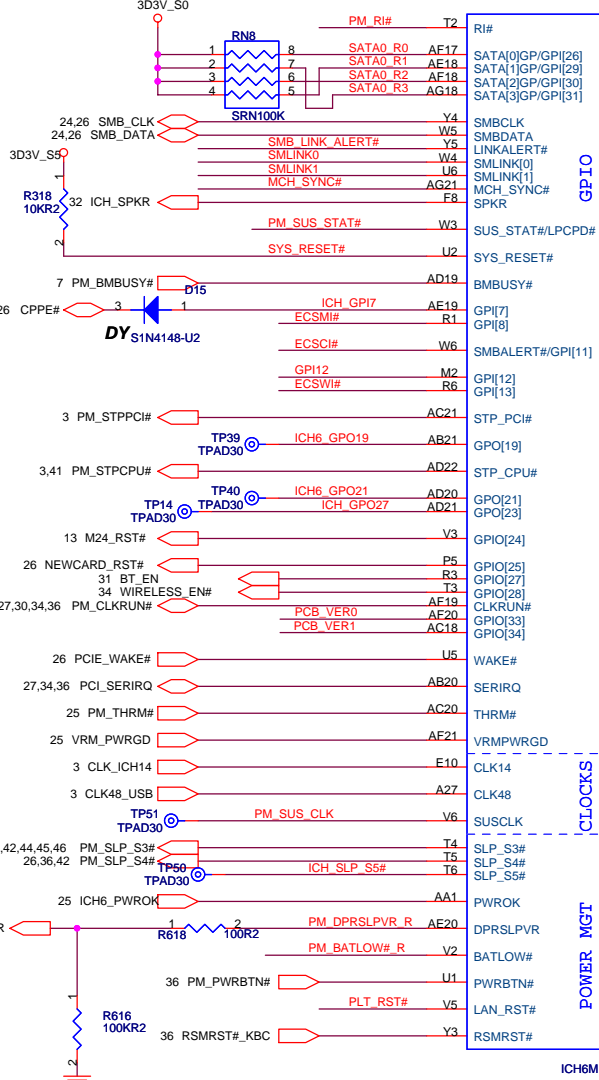
### ICH6M Pullups



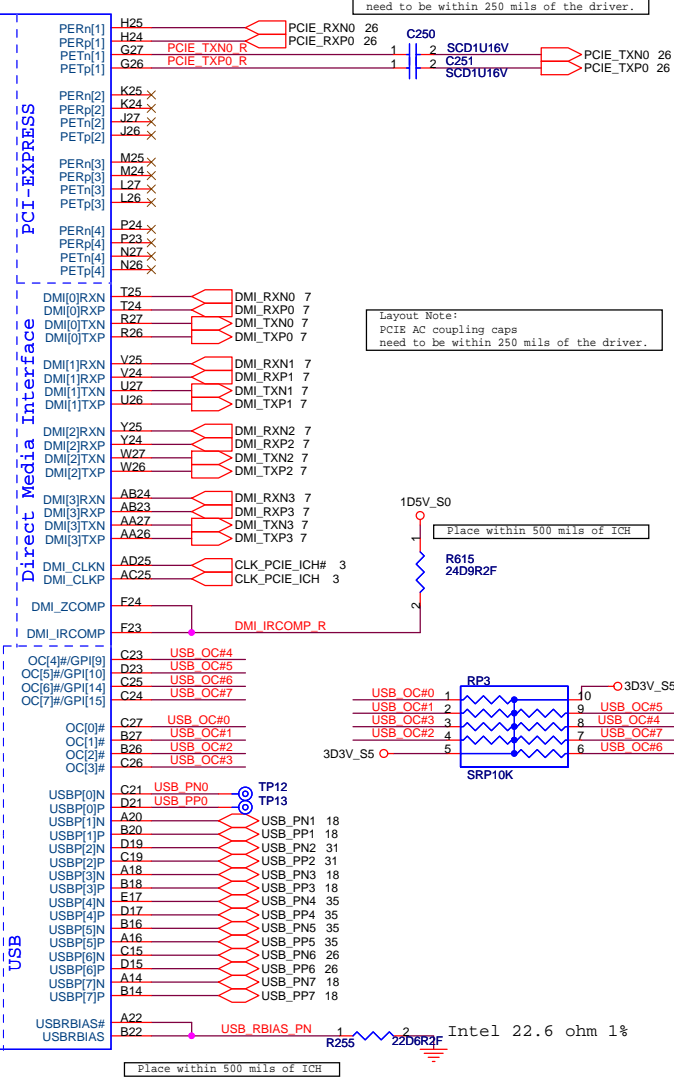
0706 -1

### PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1	PCB_VER2
SA	0	0	0
SB	0	1	0
SC	1	0	0
-1	1	1	0
-2	0	0	1



U42C

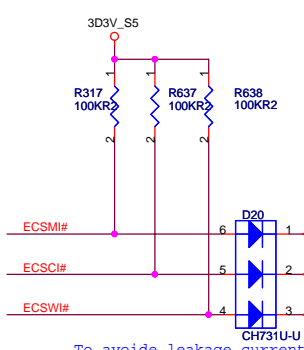


PCI AC coupling caps need to be within 250 mils of the driver.

Layout Note: PCI AC coupling caps need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500 mils of ICH



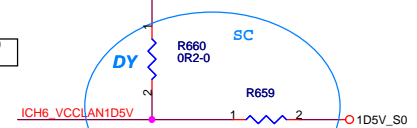
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Title: ICH6-M (2 of 4)

Size A3 Document Number Rev -1

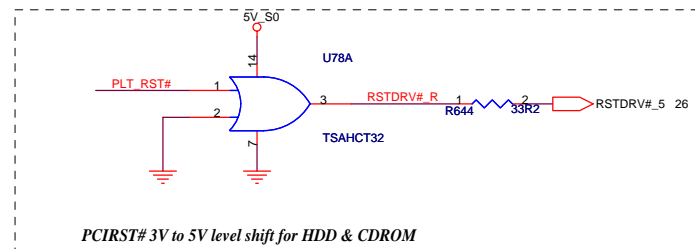
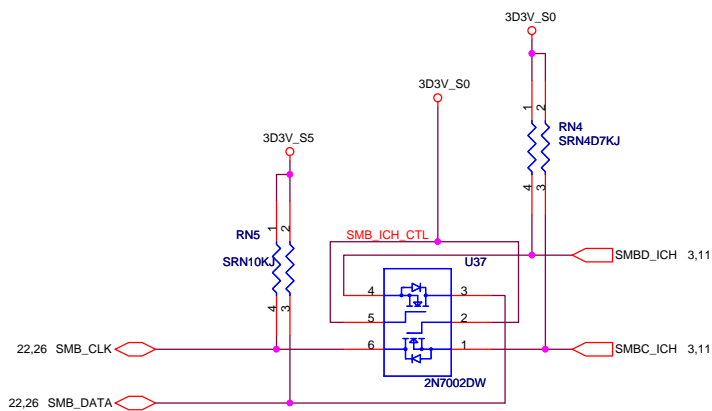
Date: Monday, July 11, 2005 Sheet 22 of 47



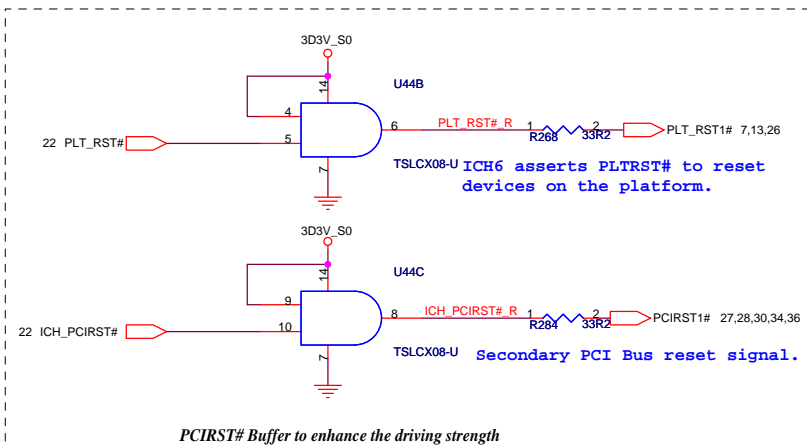
Place within 100  
miles of I  
A17

WWW.AliSaler.Com

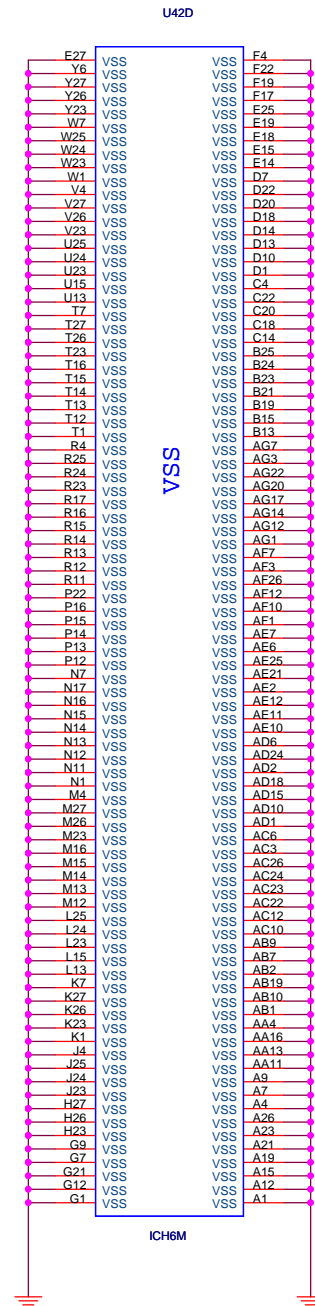
SMBUS ( ICH6 ---> SODIMM,CLKGEN )

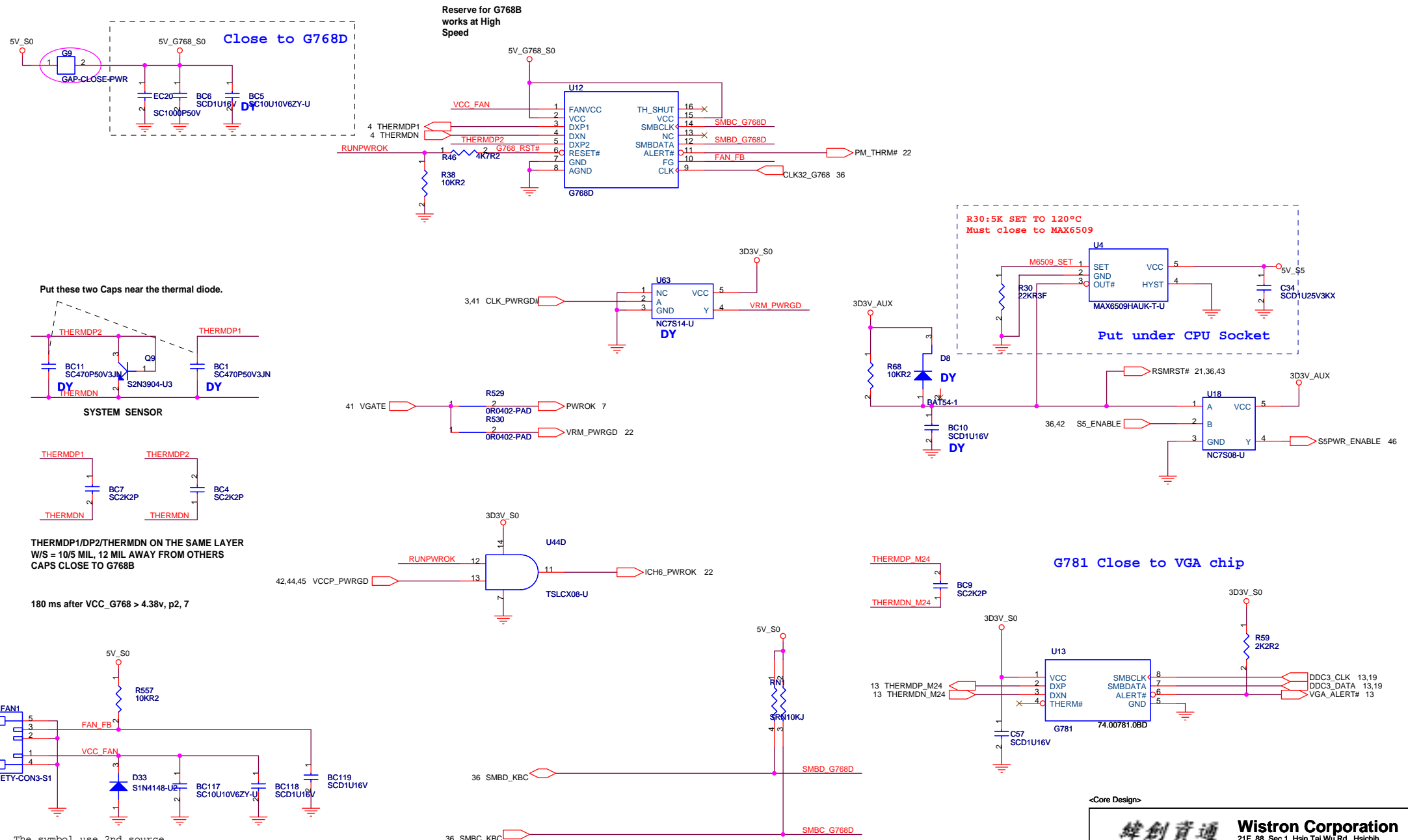


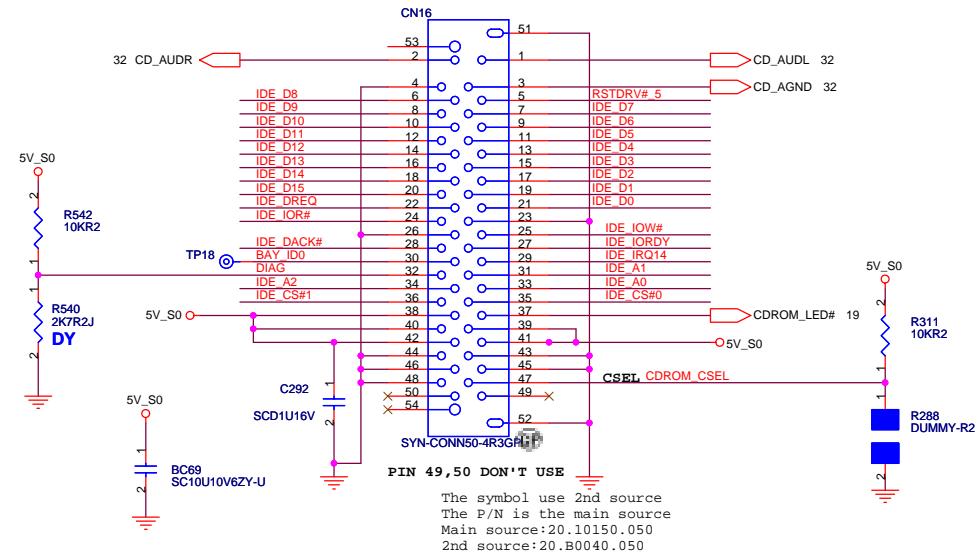
PCIRST# 3V to 5V level shift for HDD & CDROM



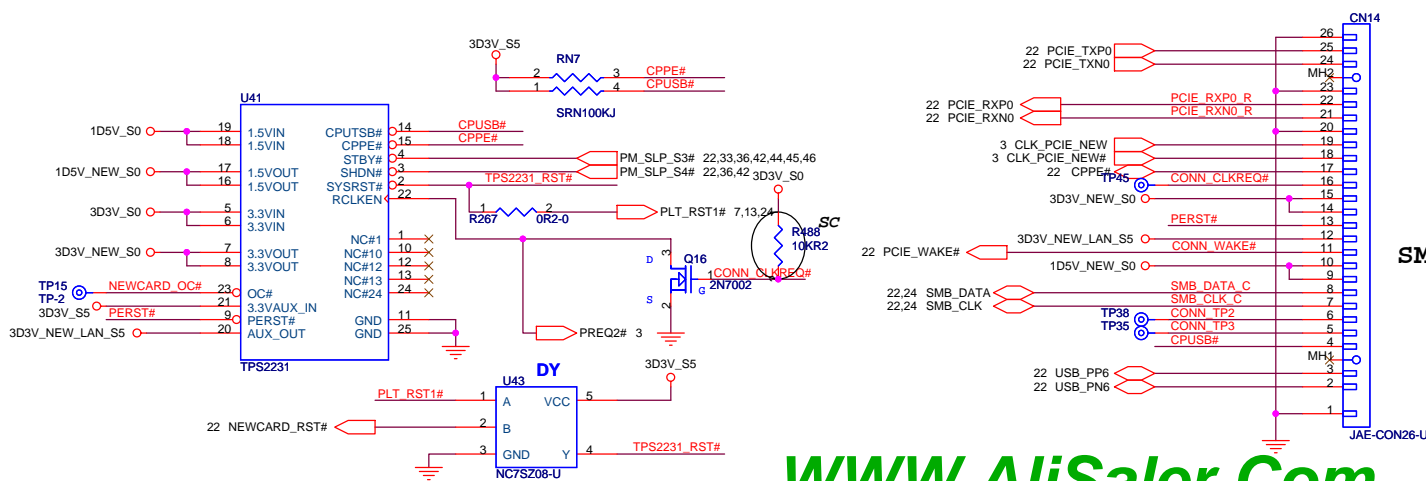
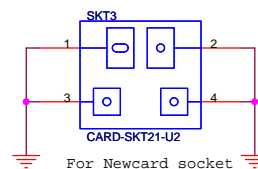
PCIRST# Buffer to enhance the driving strength







Place them Near to Connector



SMBUS ( ICH6--NEWCARD, LAN )

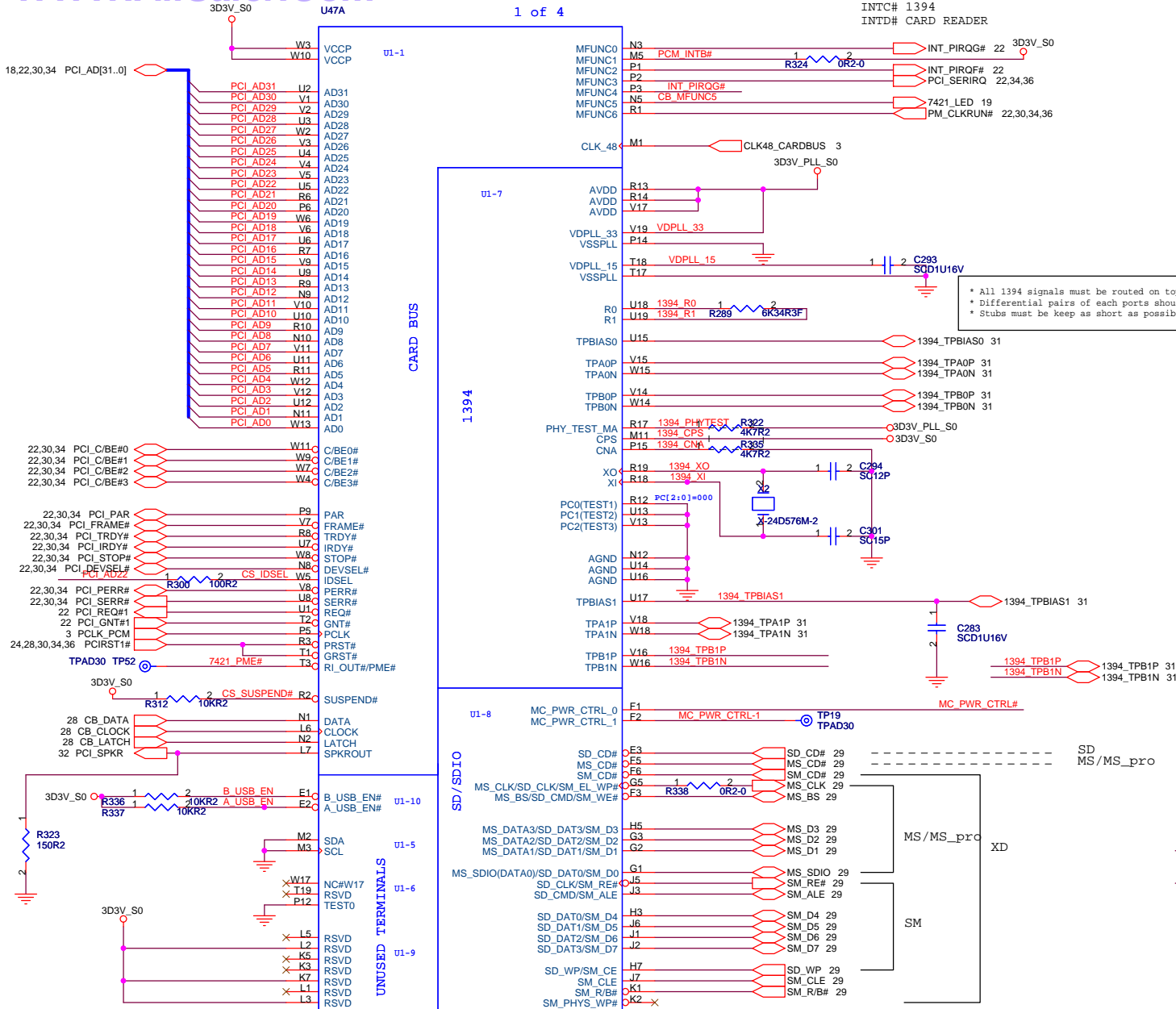
### <Core Design>

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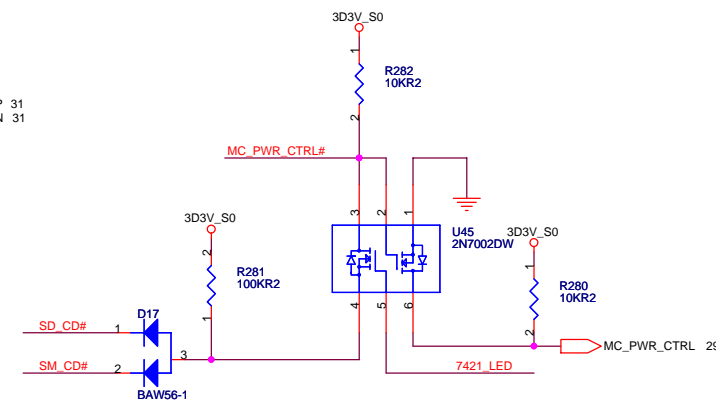
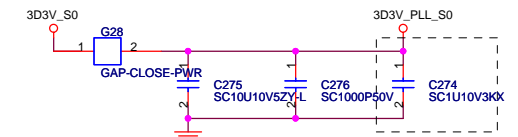
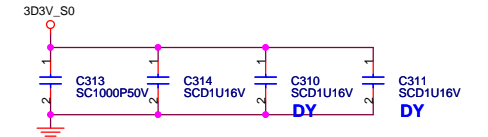
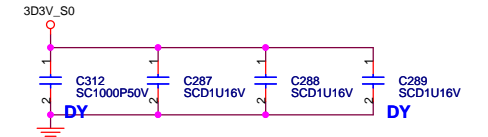
Title			
<b>HDD / CDROM/NEWCARD</b>			
Size	Document Number	Rev	
A3	Leopard2	-1	
Date:	Monday, July 11, 2005	Sheet 26	of 47



INTA# CARBUS 1  
INTB# NONE  
INTC# 1394  
INTD# CARD READER

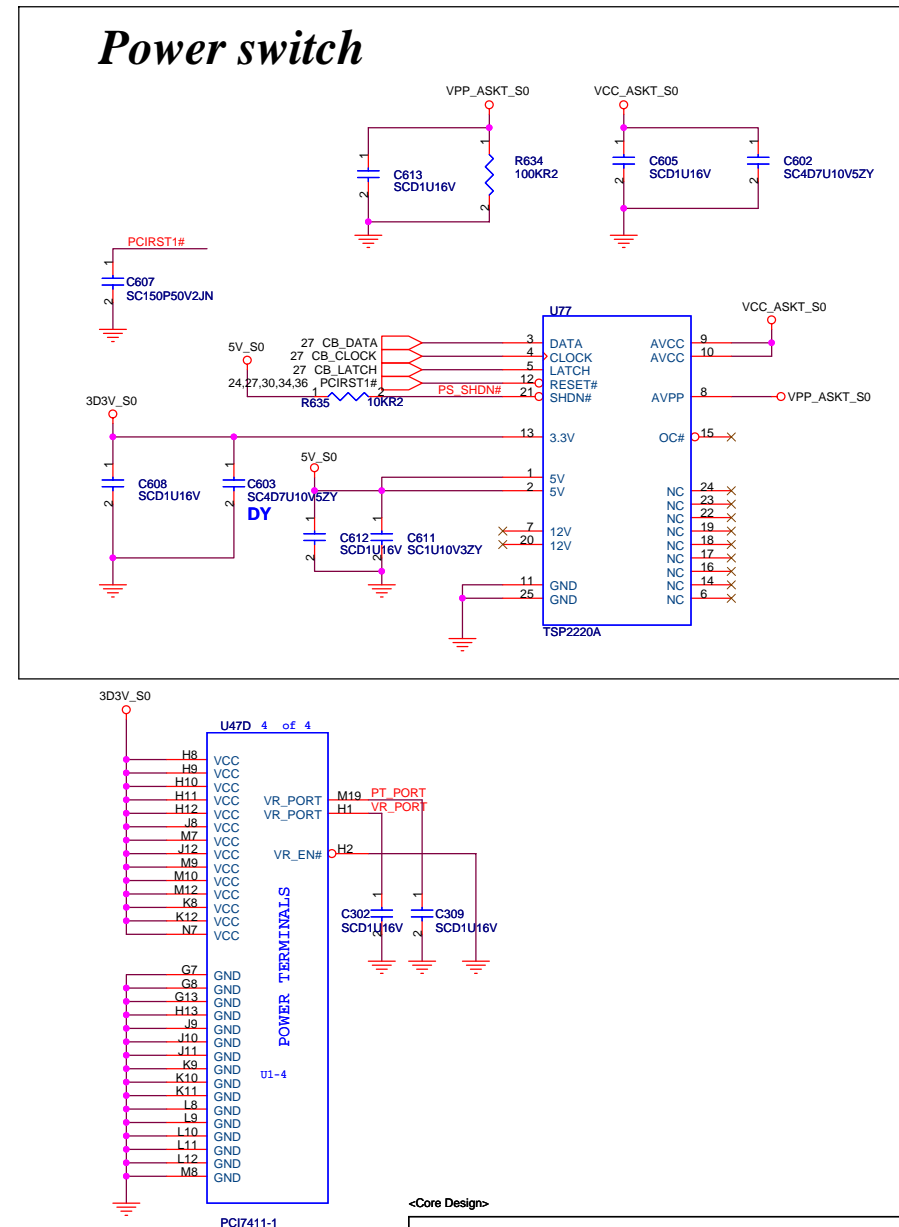


Bypass/Decoupling Capacitors  
Should be places as close to  
PCI7421 as possible



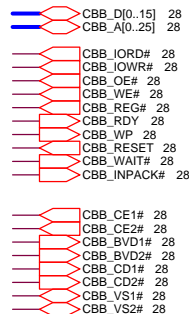
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<p>緯創資通 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title <b>TI SNC1Q21 (1 of 2)</b></p>		
Size A3	Document Number	Rev -1
Date: Monday, July 11, 2005	Sheet 27 of 47	

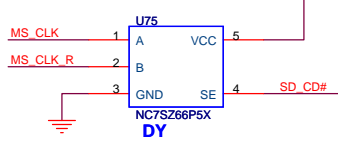
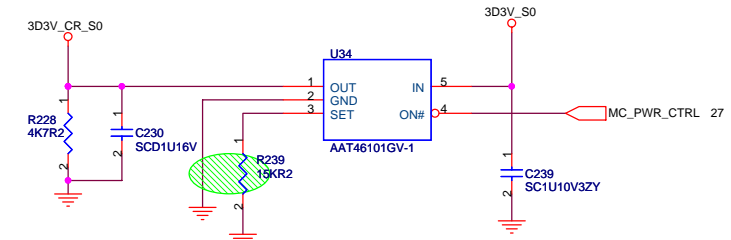
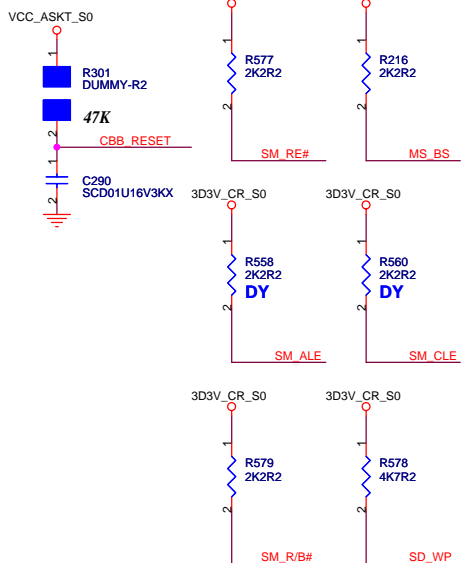
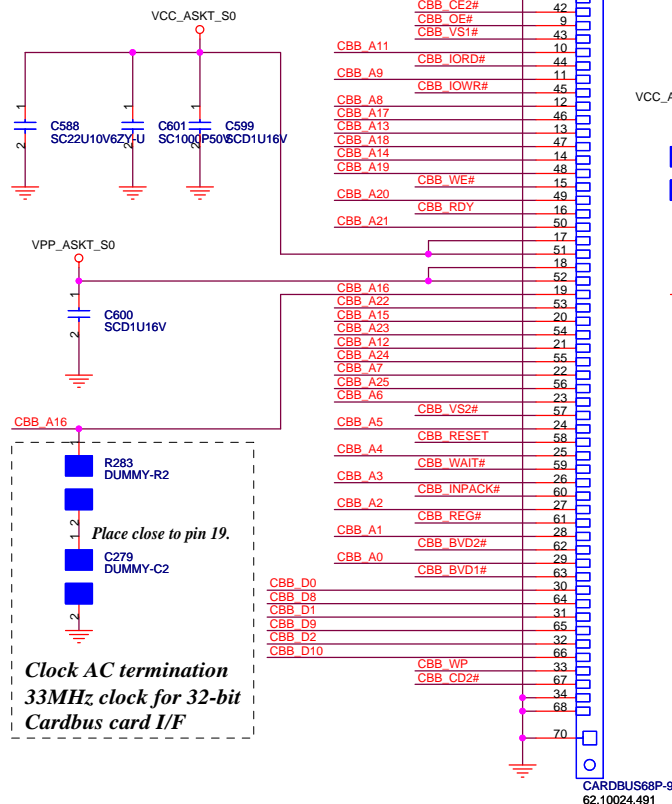
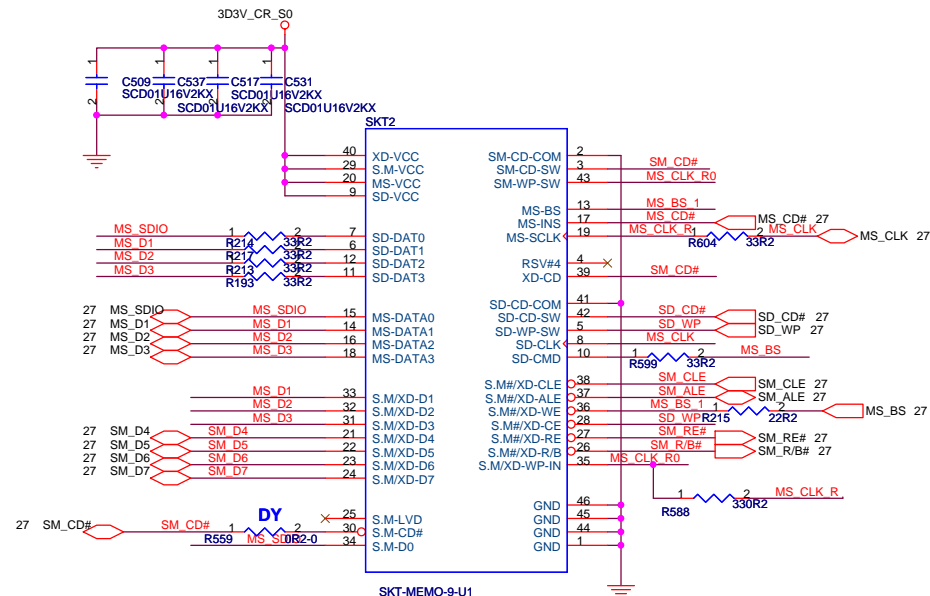


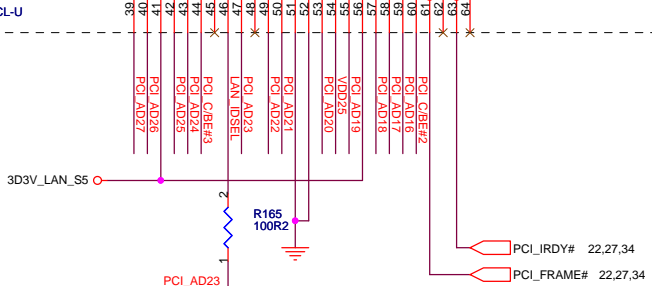
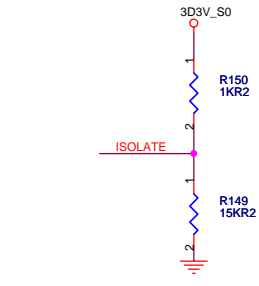
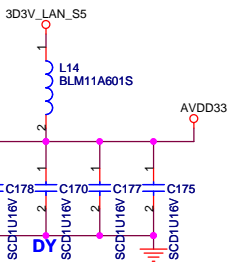
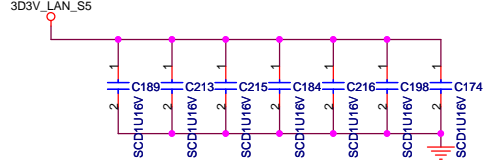
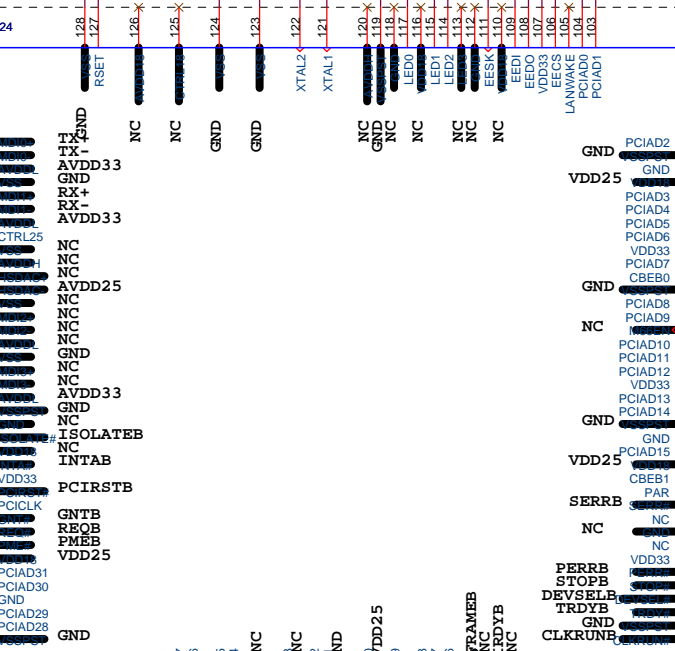
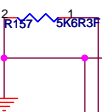
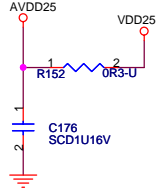
# PCMCIA Socket

## Cardbus I/F



## 6 in 1 Connector

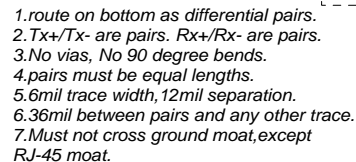




From NEW!  
1004-1



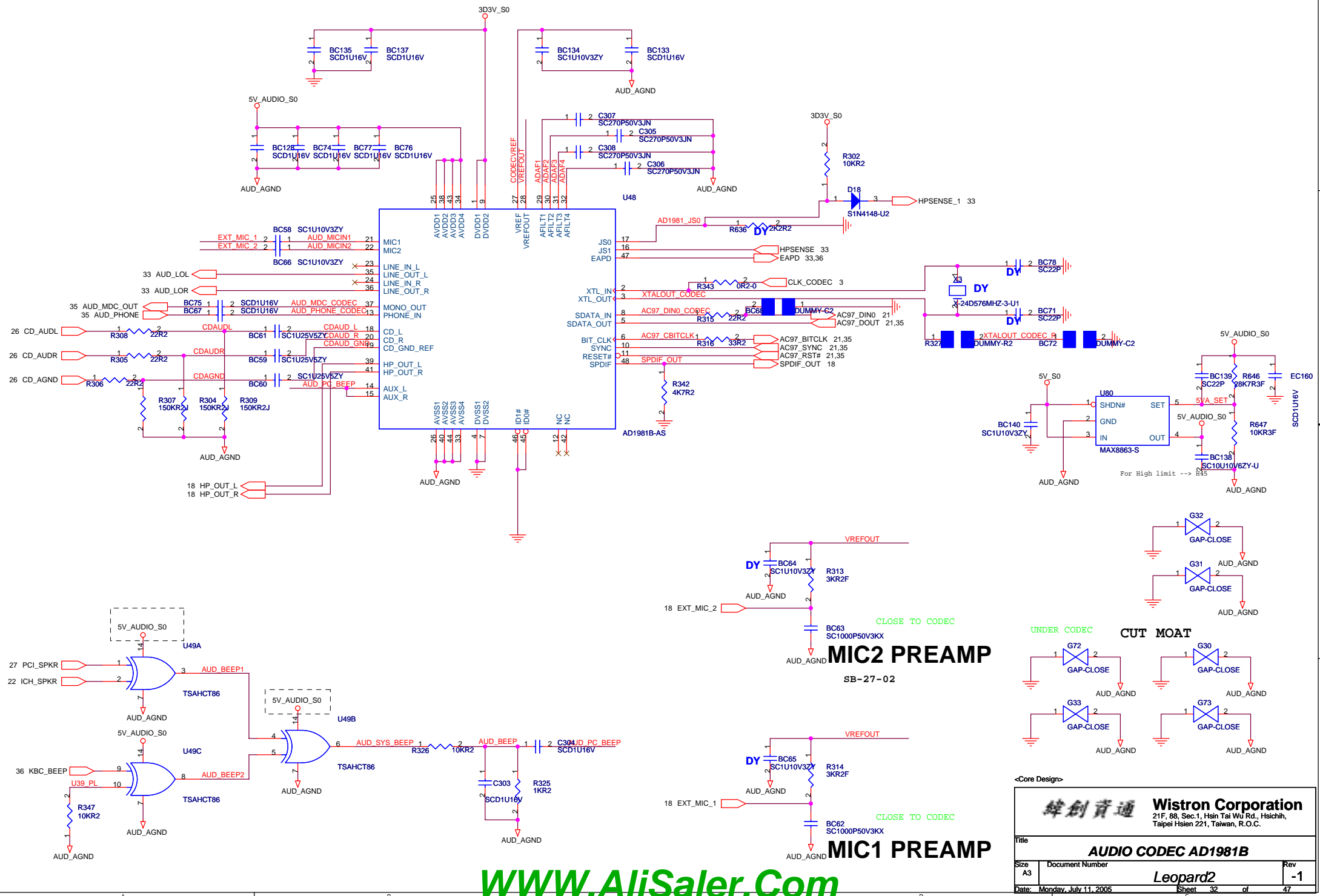
### 10/100M Lan Transformer



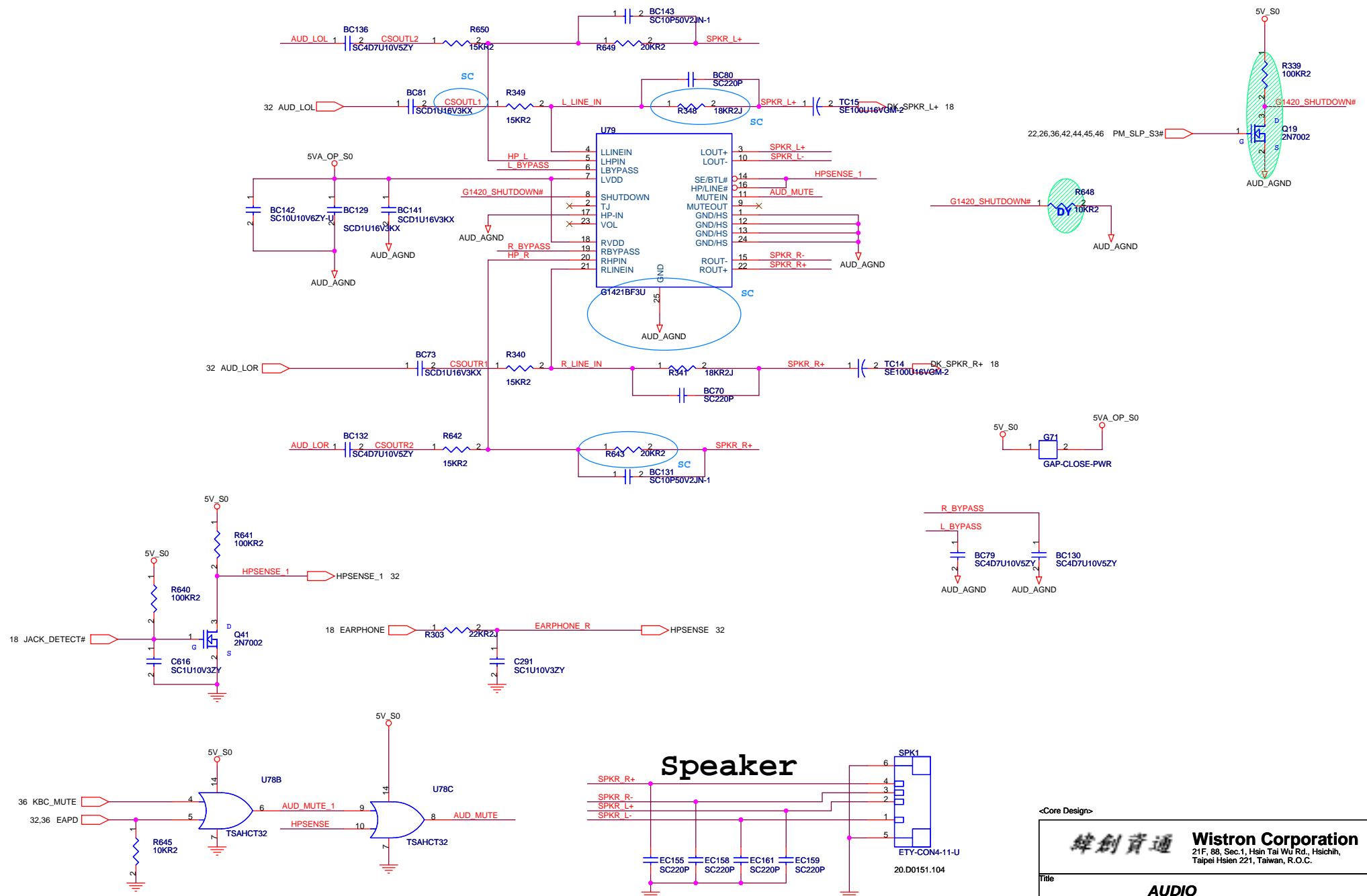
**These components near to chip side.**



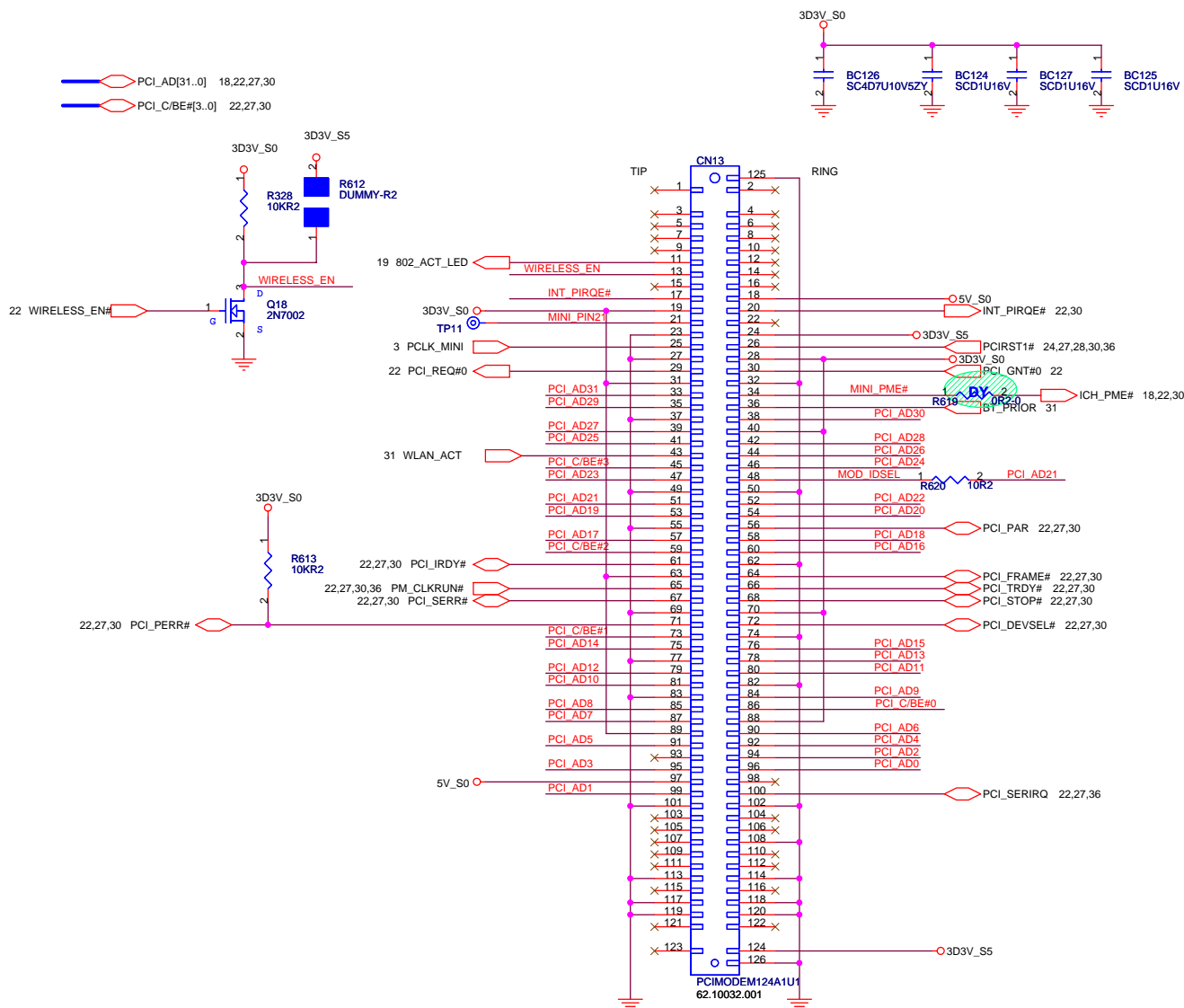
Title			
<b>LAN / 1394 Connector</b>			
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## MINI-PCI



```
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031
```

### <Core Design>

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A3

Document Number
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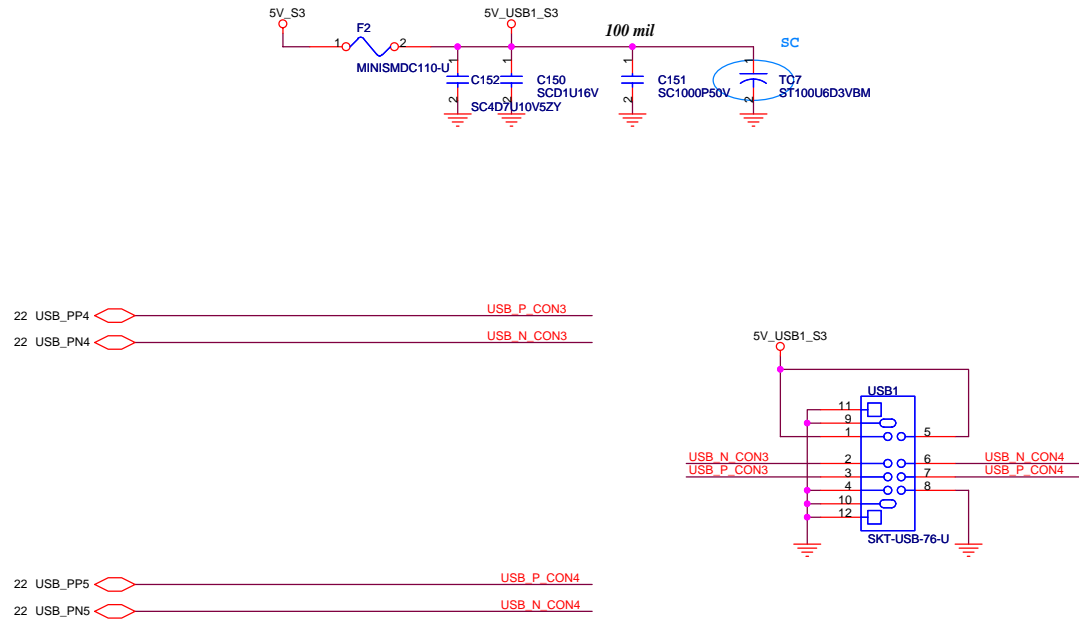
Leopard2

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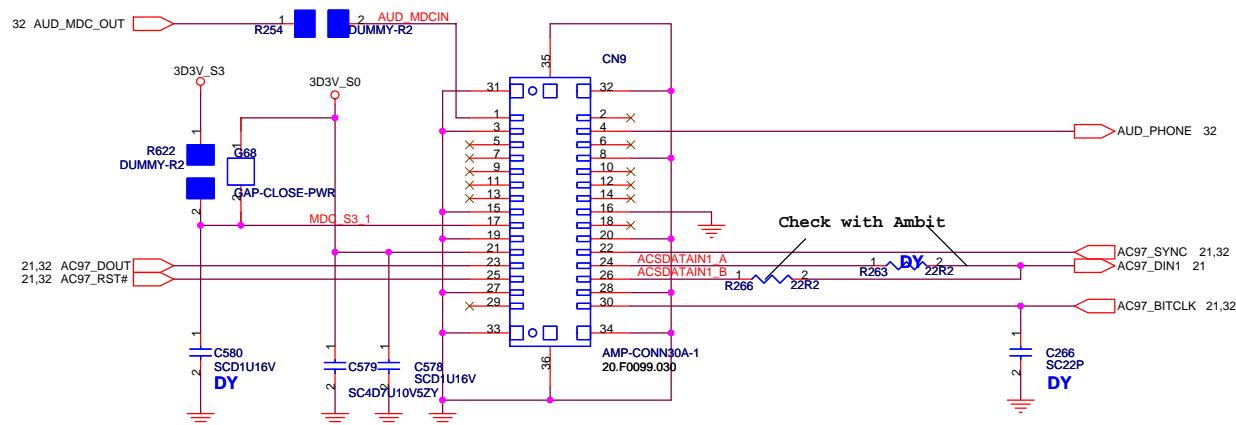
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## USB POWER



## *MDC Connector*



**<Core Design>**

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**USB / MDC CONN.**Size  
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Title

**KBC NS97551**

Size

Document Number

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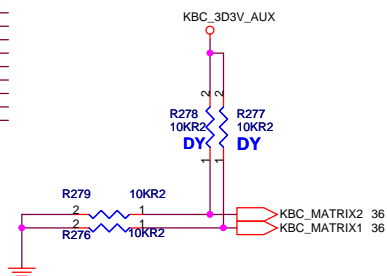
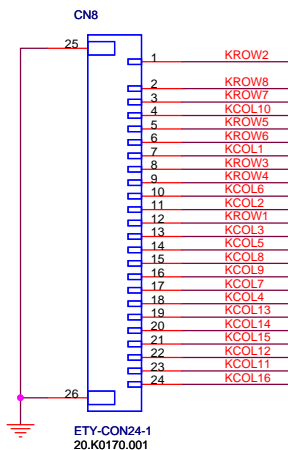
47

SHM=1: Enable shared memory with host BIOS  
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+
1 1	Reserved	

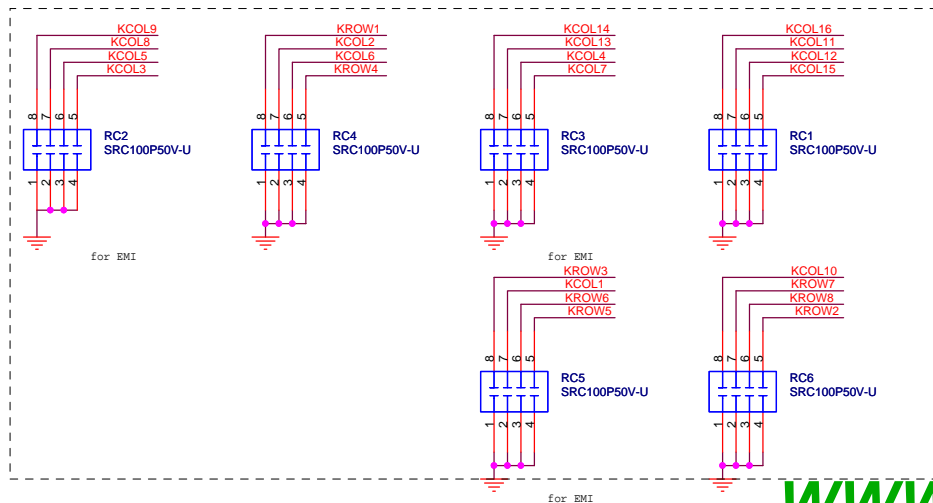
# INTERNAL KEYBOARD CONNECTOR

KROW[1..8] 36 KCOL[1..16] 36



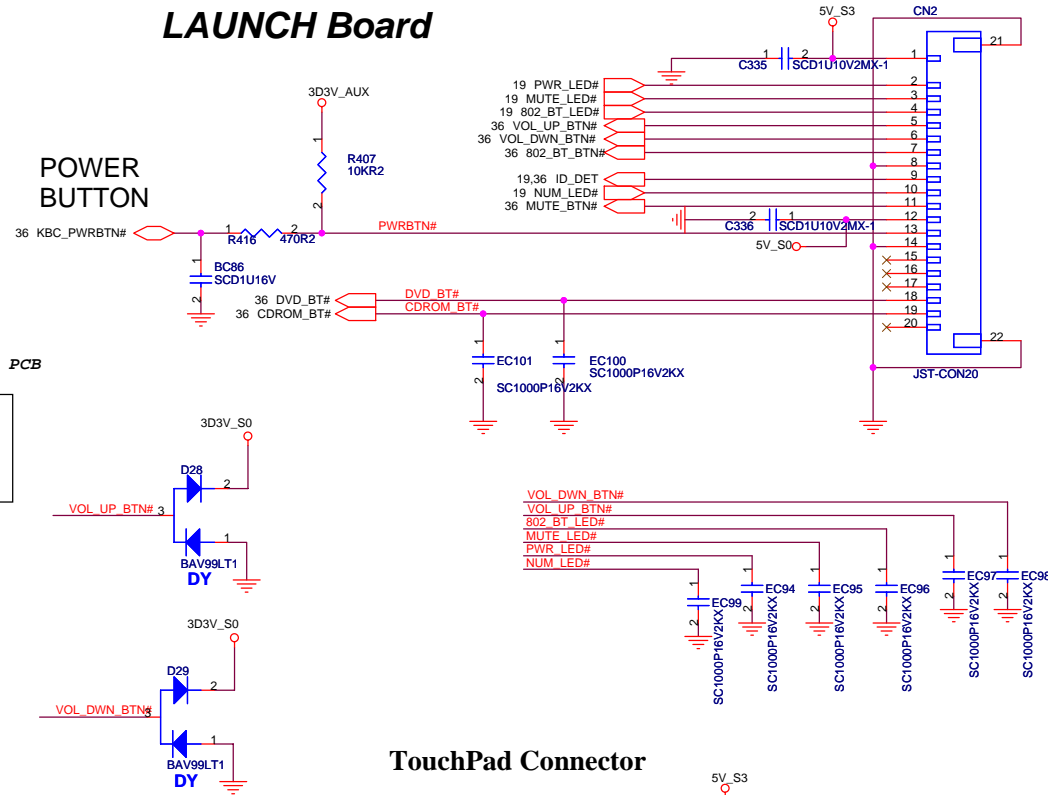
the matrix table for PCB

	PA	PR
Discrete	00	01
UMA	10	11

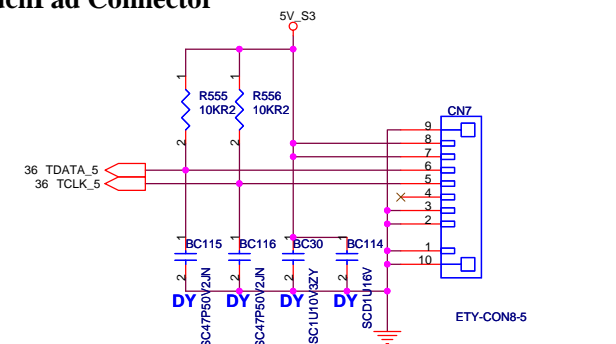


## LAUNCH Board

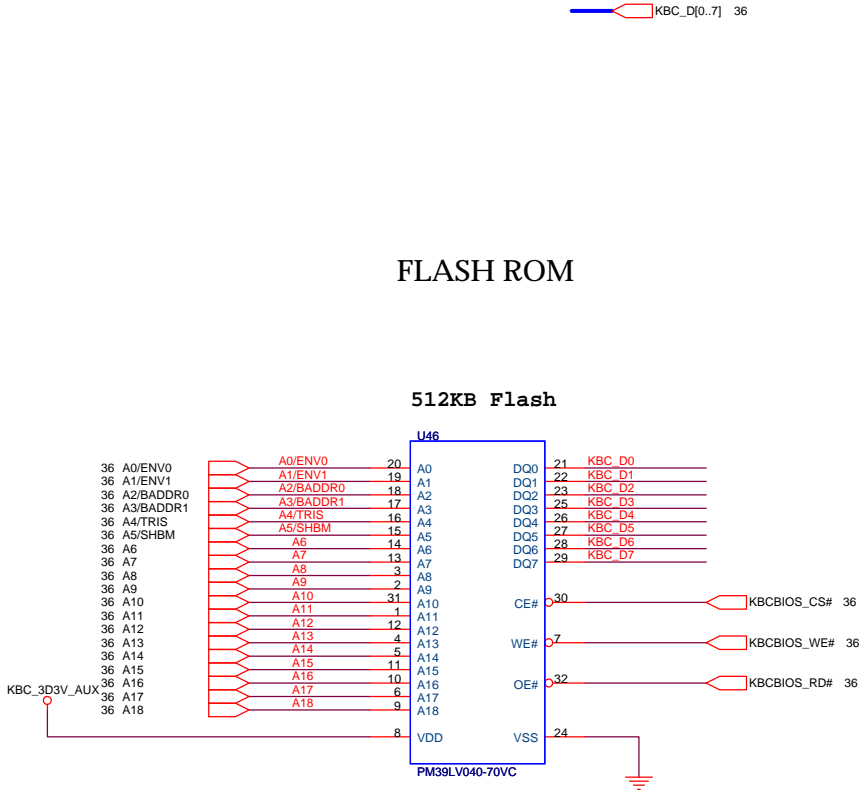
### POWER BUTTON



### TouchPad Connector



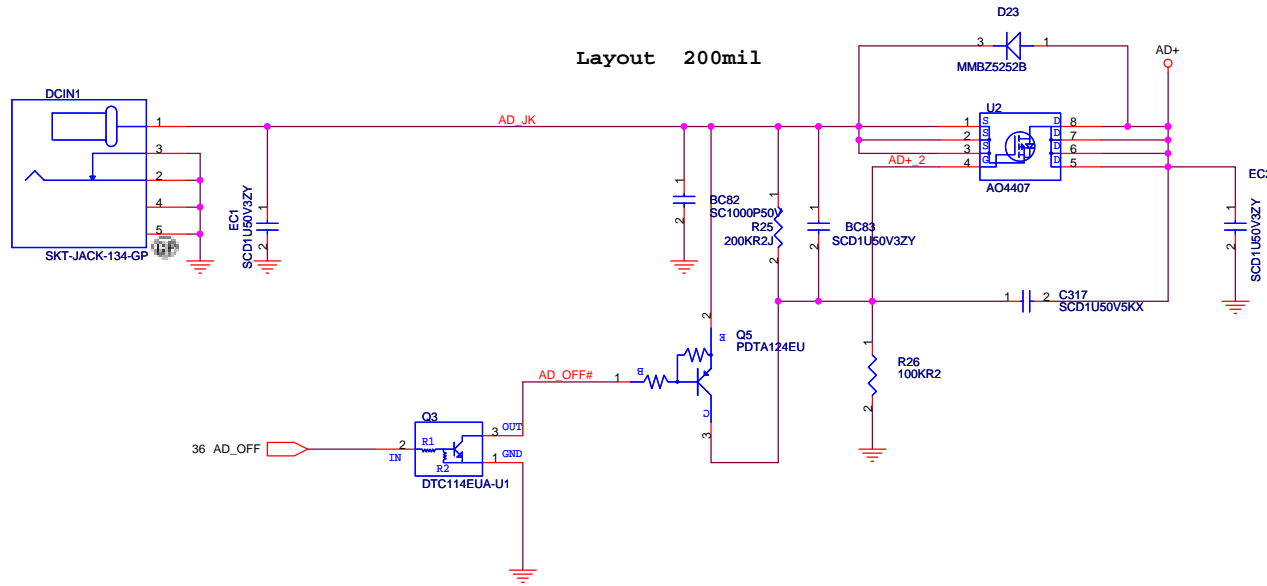
<Core Design>



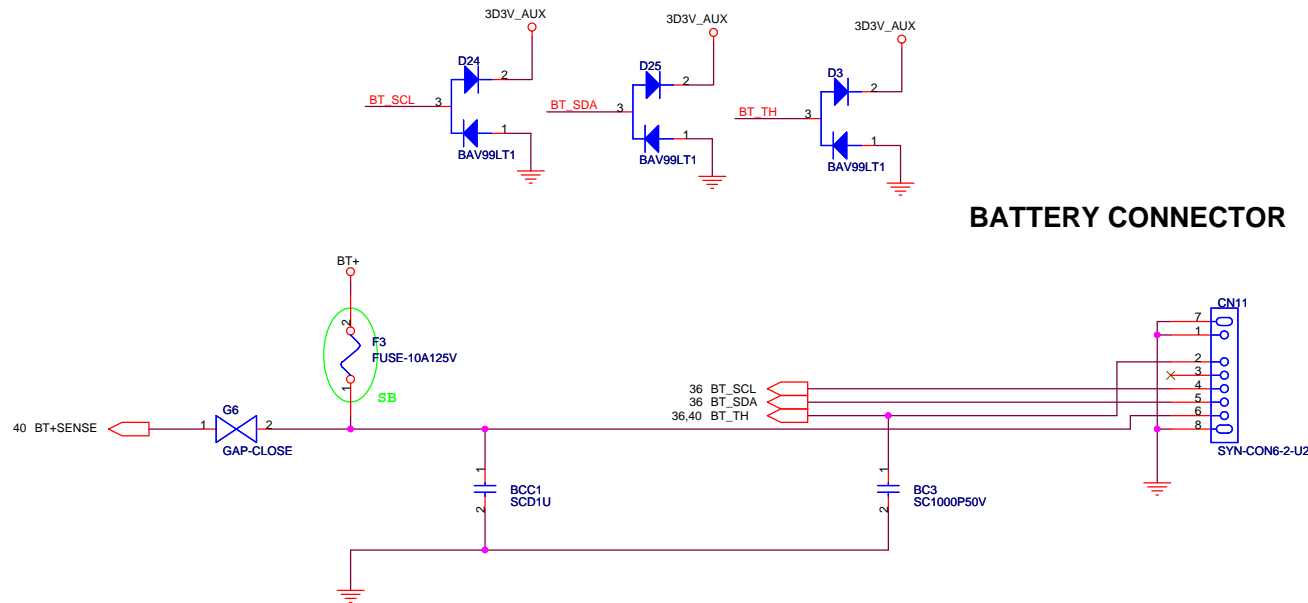


# Adaptor in to generate DCBATOUT

Layout 200mil



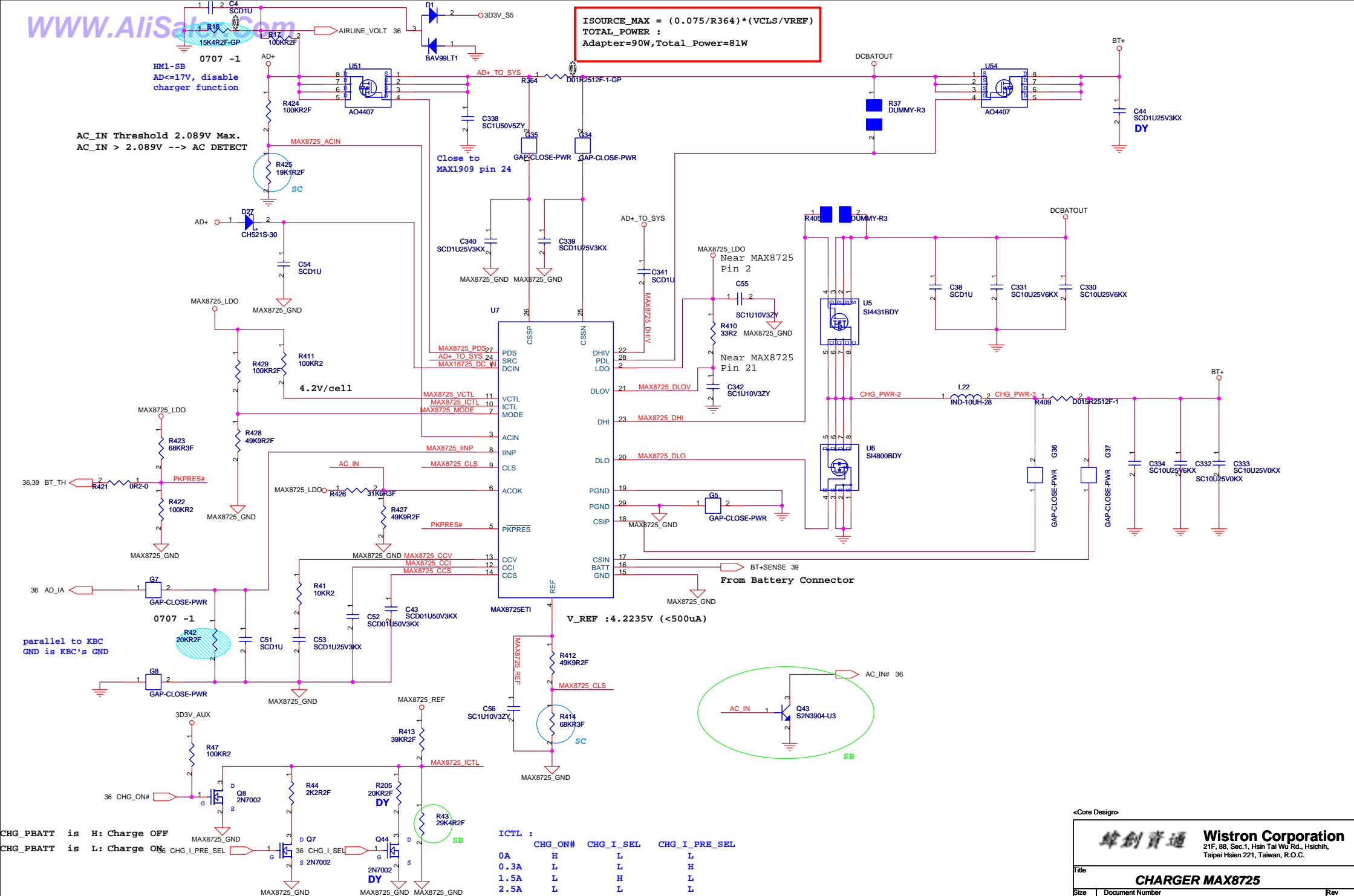
## BATTERY CONNECTOR



<Core Design>

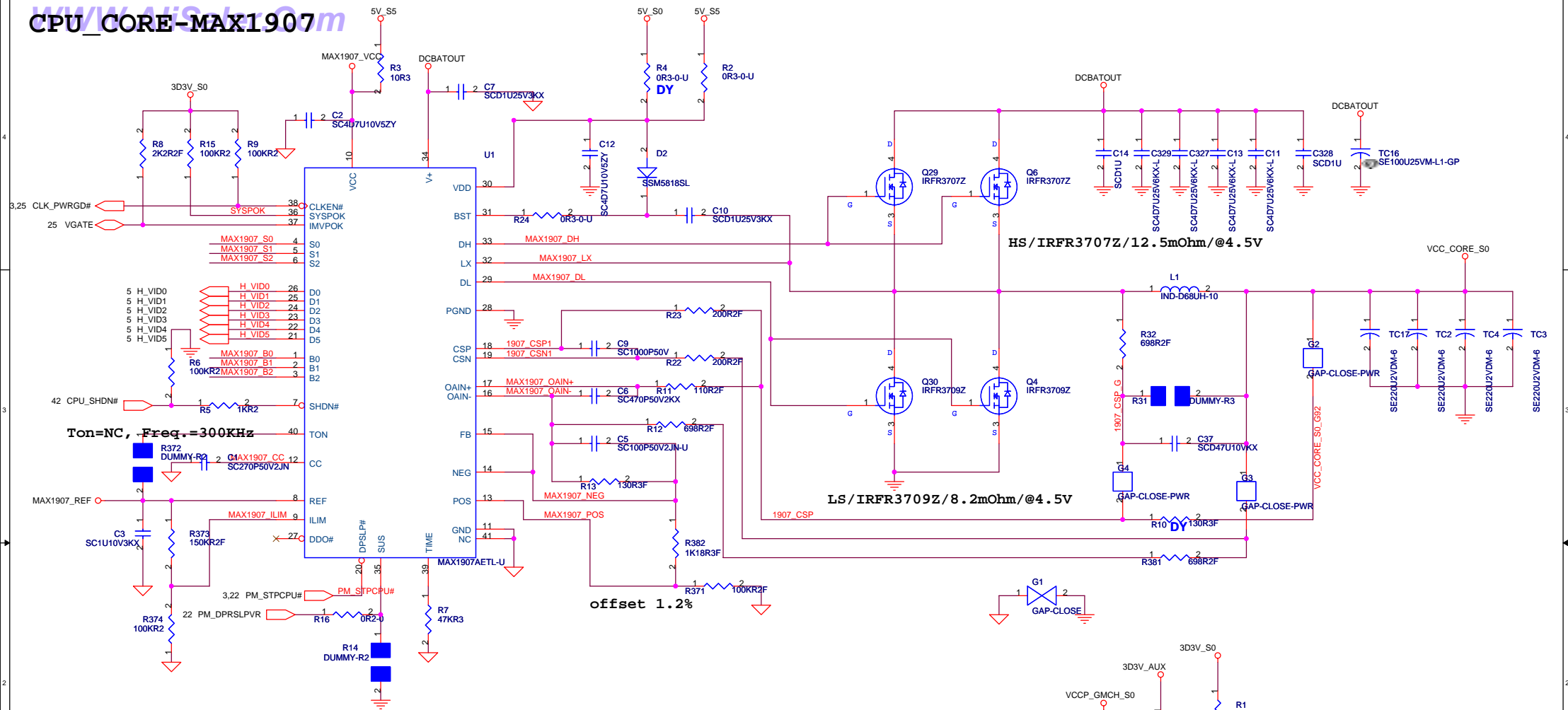
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Title			Adaptor/ Battery conn.	
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If Charger is MAX1909,dummy them.

## CPU\_CORE-MAX1907

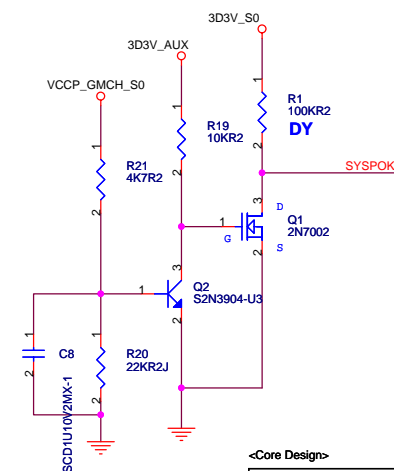


OCP=30A, Vally current = 27.5A,  
Vilim=550mV(55mVp-p\*10)

Deeper Sleep Voltage : 0.748V  
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V  
 , B0=L, B1=L, B2=Open

VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.34
0	1	1	0	0	0	1.32
0	1	1	0	1	0	1.29
0	1	1	1	0	0	1.26
0	1	1	1	0	1	1.24
0	1	1	1	1	1	1.21
1	0	0	0	0	1	1.18
1	0	0	0	1	1	1.14
1	0	0	1	1	0	1.10
1	0	1	0	0	1	1.05
1	0	1	0	1	1	1.02
1	0	1	1	1	0	0.97
1	1	0	0	0	0	0.94



**<Core Design>**

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Title			
<b><i>IMVP IV-CPU POWER-MAX1907</i></b>			
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# TI TPS5130 for 1D8V, 3D3V, 5V

For 3.3V  
SETTING=3.349V

(1D8V=>CH1 , 3D3V=>CH2 , 5V =>CH3)

For 5V  
SETTING=5.0915V

1D8V\_OCP

3D3V\_OCP

5V\_OCP

$$V_o = (R1 * 0.85) / R2 + 0.85$$

TPS5130

	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	L : PWM fixed (300KHz)	~0.3V(Max)

<Core Design>

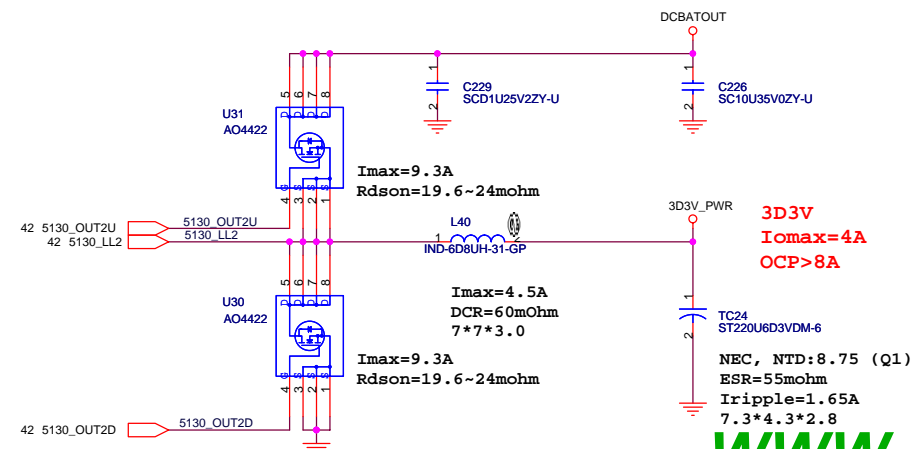
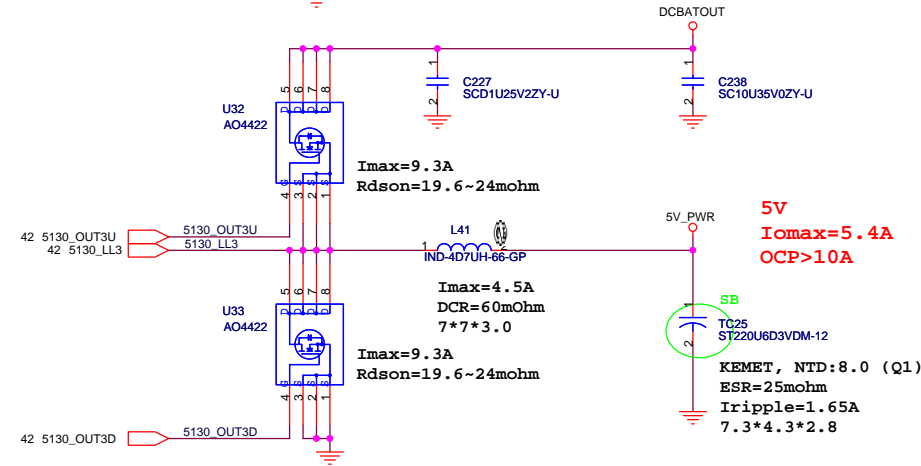
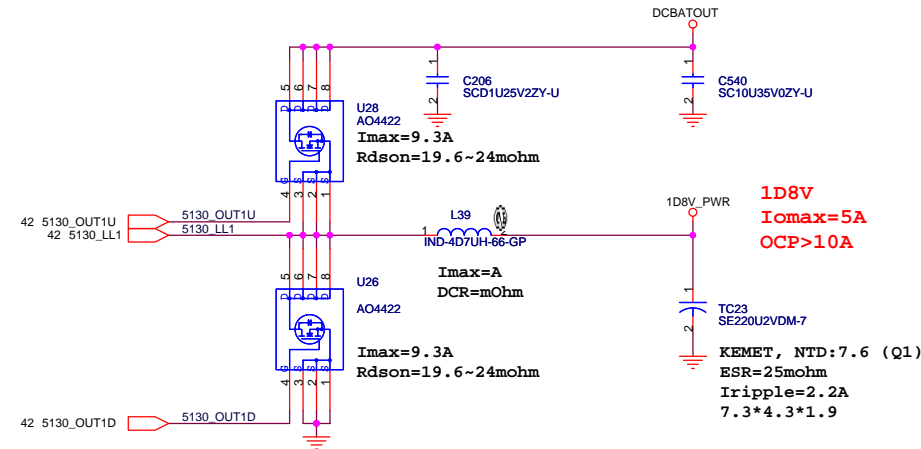
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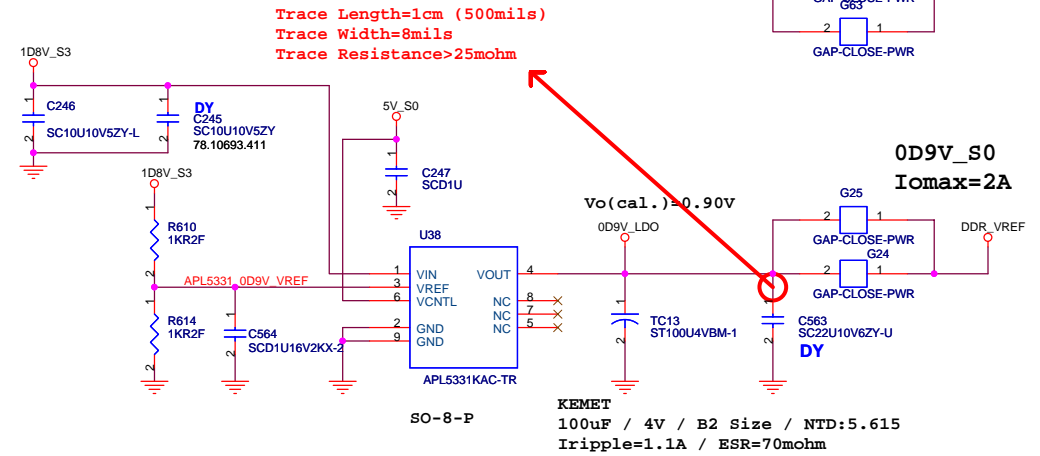
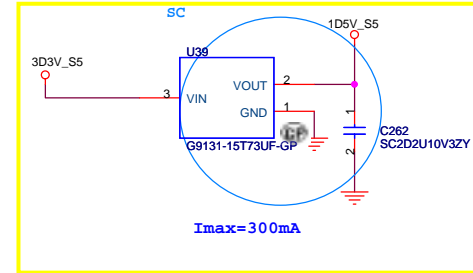
Title			
TPS5130 (3D3V/5V/1D8V)			
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# TI TPS5130 for 1D2V, 5V, 3D3V

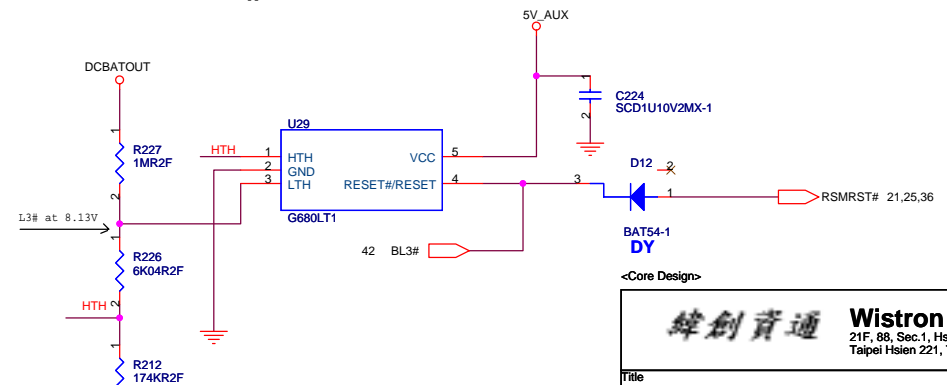
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)

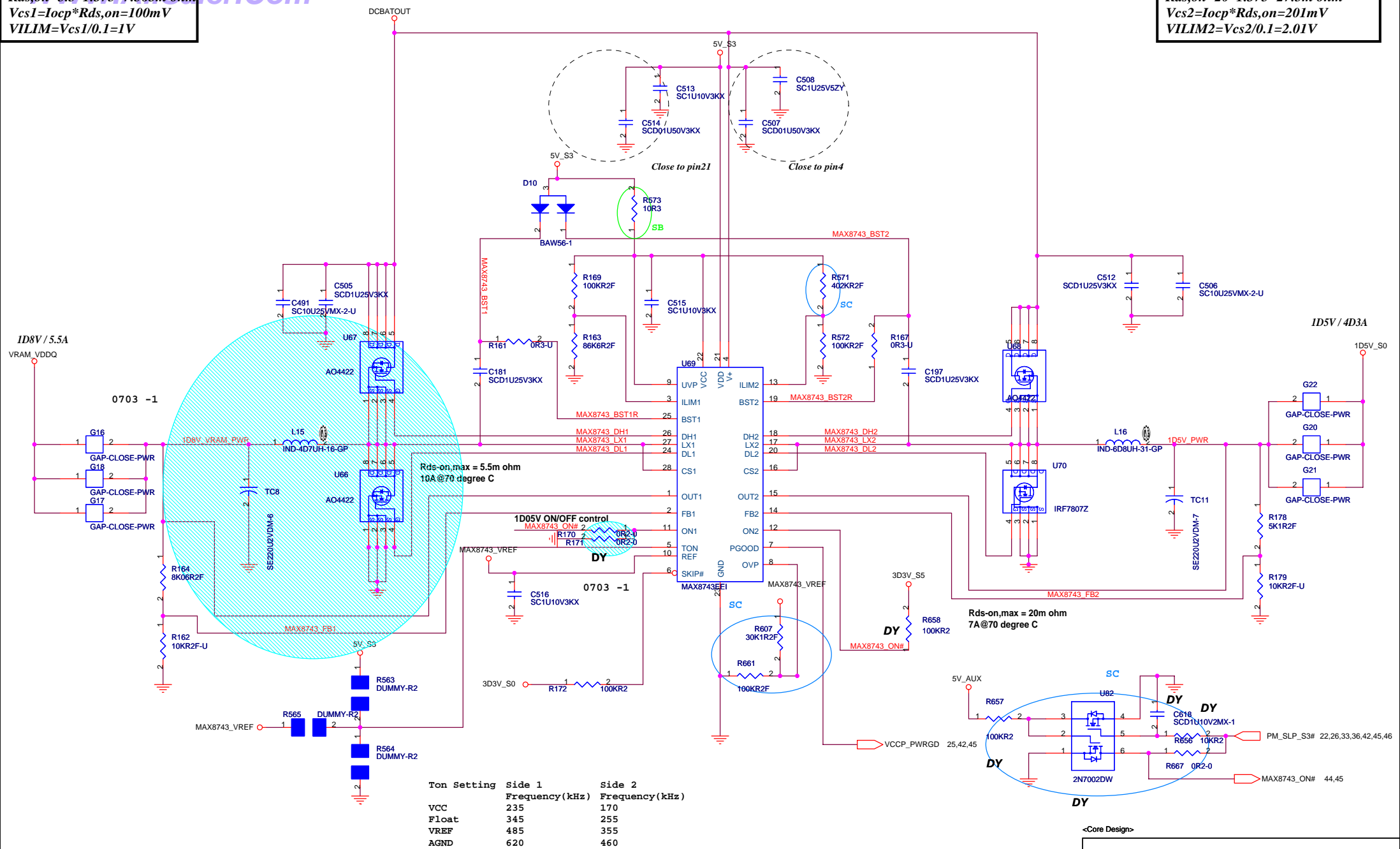


## 1.5V\_S5 (For ICH6)



## L3# circuit



$$\begin{aligned} I_{ocp} &= 7.8 * 1.7 = 13.3A \\ R_{ds,on} &= 5.5 * 1.375 = 7.563m\ \Omega \\ V_{cs1} &= I_{ocp} * R_{ds,on} = 100mV \\ V_{ILIM} &= V_{cs1} / 0.1 = 1V \end{aligned}$$
$$\begin{aligned} I_{ocp} &= 4.3 * 1.7 = 7.3A \\ R_{ds,on} &= 20 * 1.375 = 27.5m\ ohm \\ V_{cs2} &= I_{ocp} * R_{ds,on} = 201mV \\ V_{ILIM2} &= V_{cs2} / 0.1 = 2.01V \end{aligned}$$


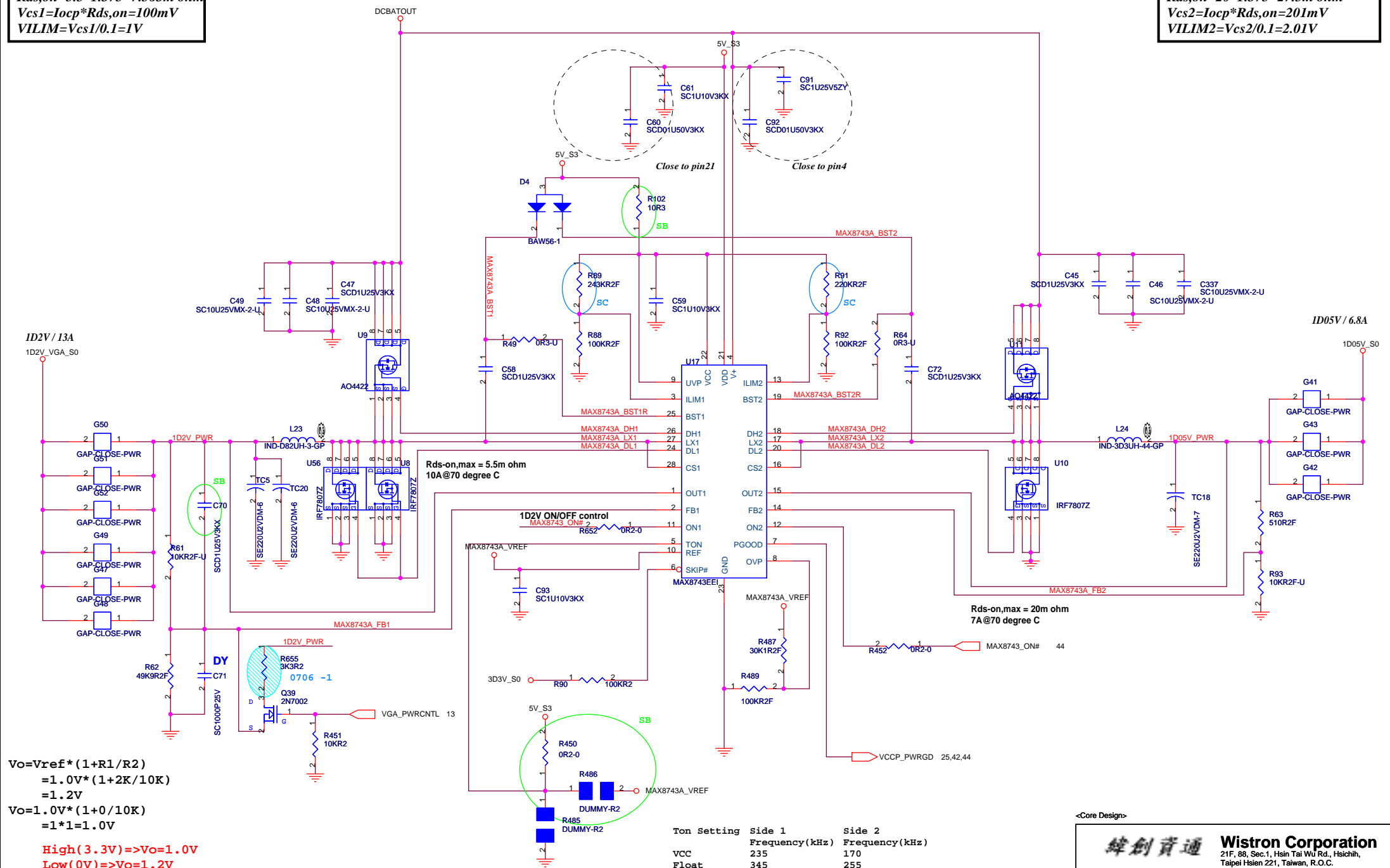
**<Core Design>**

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Title	<b>MAX8743 (1D8V_S0/1D5V_S0)</b>
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$$\begin{aligned} I_{ocp} &= 4.3 * 1.7 = 7.3A \\ R_{ds,on} &= 20 * 1.375 = 27.5m\ ohm \\ V_{cs2} &= I_{ocp} * R_{ds,on} = 201mV \\ V_{ILIM2} &= V_{cs2} / 0.1 = 2.01V \end{aligned}$$


M24/M26 POWER PLAY (VGA\_PWRCNTL)  
high (3.3V) = set lower core voltage (VDDC = 1.0V)  
low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1	Side 2
	Frequency(kHz)	Frequency(kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

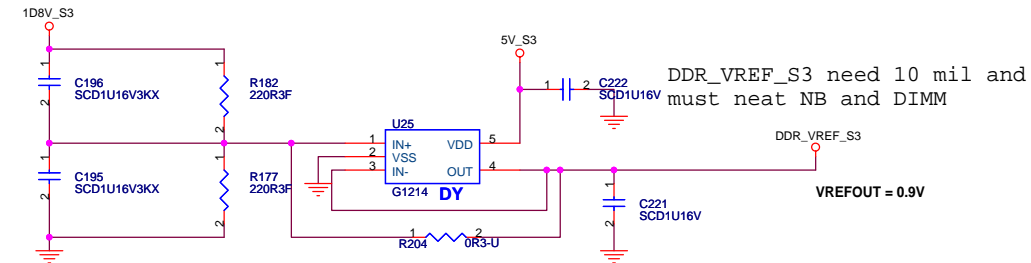
&lt;Core Design&gt;

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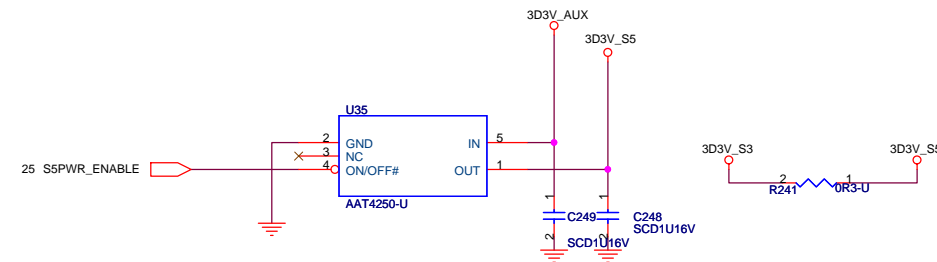
Title	<b>MAX8743 (1D2V_VGA_S0/1D05V)</b>
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FOR DDR2 Power

Suspend Power



Run Power

